Challenges and Opportunities of Technologies and Components for Diversified Future Silicon Platforms

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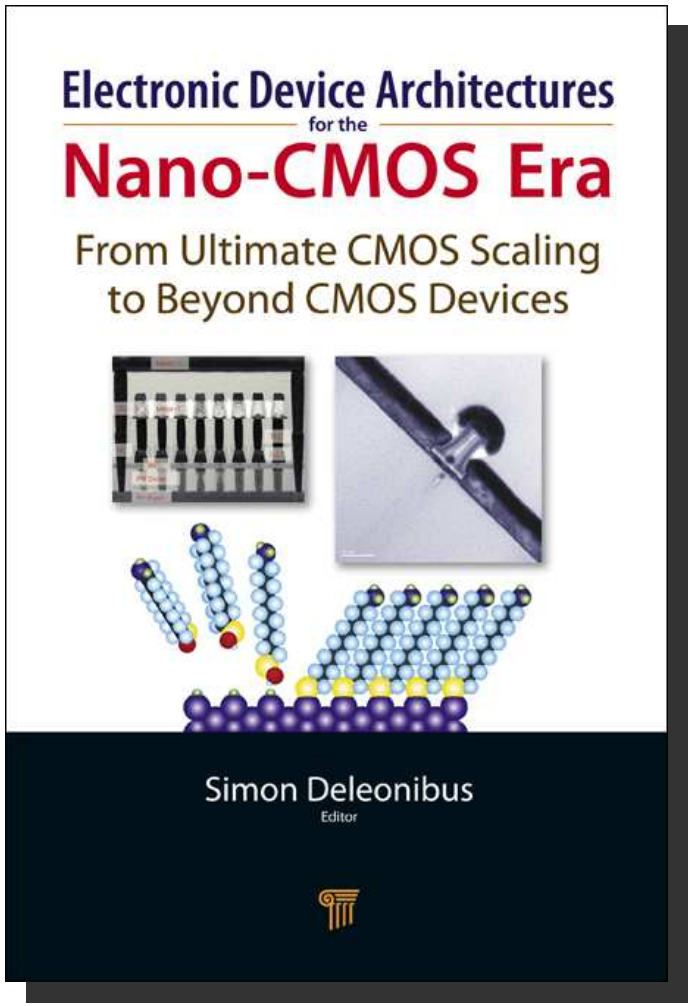


Available at Amazon.com or any good bookstores.

Electronic Device Architectures for the Nano-CMOS Era

From Ultimate CMOS Scaling to Beyond CMOS Devices

edited by Simon Deleonibus **(*CEA-LETI, France*)**

Cloth July 2008 978-981-4241-28-1

★ Discusses the scaling limits of CMOS, the leverage brought by new materials, processes and device architectures (HiK and metal gate, SOI, GeOI, Multigate transistors, and others), the fundamental physical limits of switching based on electronic devices and new applications based on few electrons operation

★ Weighs the limits of copper interconnects against the challenges of implementation of optical interconnects

★ Reviews different memory architecture opportunities through the strong low-power requirement of mobile nomadic systems, due to the increasing role of these devices in future circuits

★ Discusses new paths added to CMOS architectures based on single-electron transistors, molecular devices, carbon nanotubes, and spin electronic FETs

PAN STANFORD PUBLISHING

www.panstanford.com

Outline

- **Introduction**
- **Nanoelectronics scaling with thin films devices, new materials and new devices architectures. Exploitation of 3rd dimension.**
- **Heterogeneous Co-integration of More Moore and More than Moore.** 3D as a strong asset. New applications .New progress laws.
- **Conclusion**

Ecological Footprint of ICTs

reported by Intergovernmental Panel Climate Change(IPCC)

Source: TU Dresden



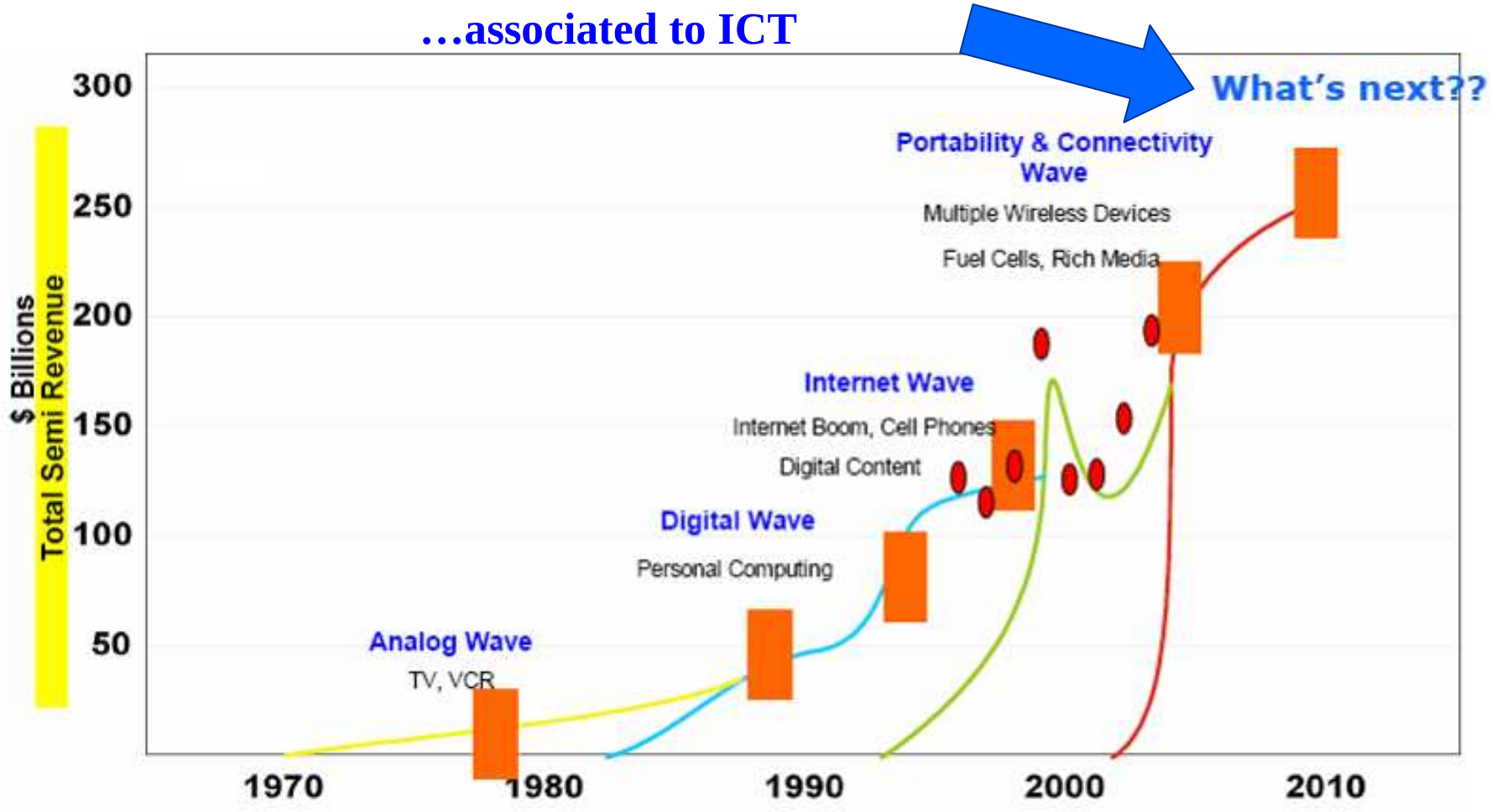
- **Currently, 3 % of the world-wide energy is consumed by the ICT infrastructure**
  - which causes about 2 % of the world-wide CO2 emissions
  - comparable to the world-wide CO2 emissions by airplanes or ¼ of the world-wide CO2 emissions by cars
- **ICT: 10% of electrical energy in industrialized nations**
  - 900 Bill.. kWh / year = Central and South Americas
- **The transmitted data volume increases approximately by a factor of 10 every 5 years**

For ICTs, keep in mind (ITRS LSTP, LOP GP, HP):

$$P = P_{stat} + P_{dyn} \qquad P_{stat} = V_{dd} x I_{off} \text{ and } P_{dyn} = C V_{dd}^2 f$$

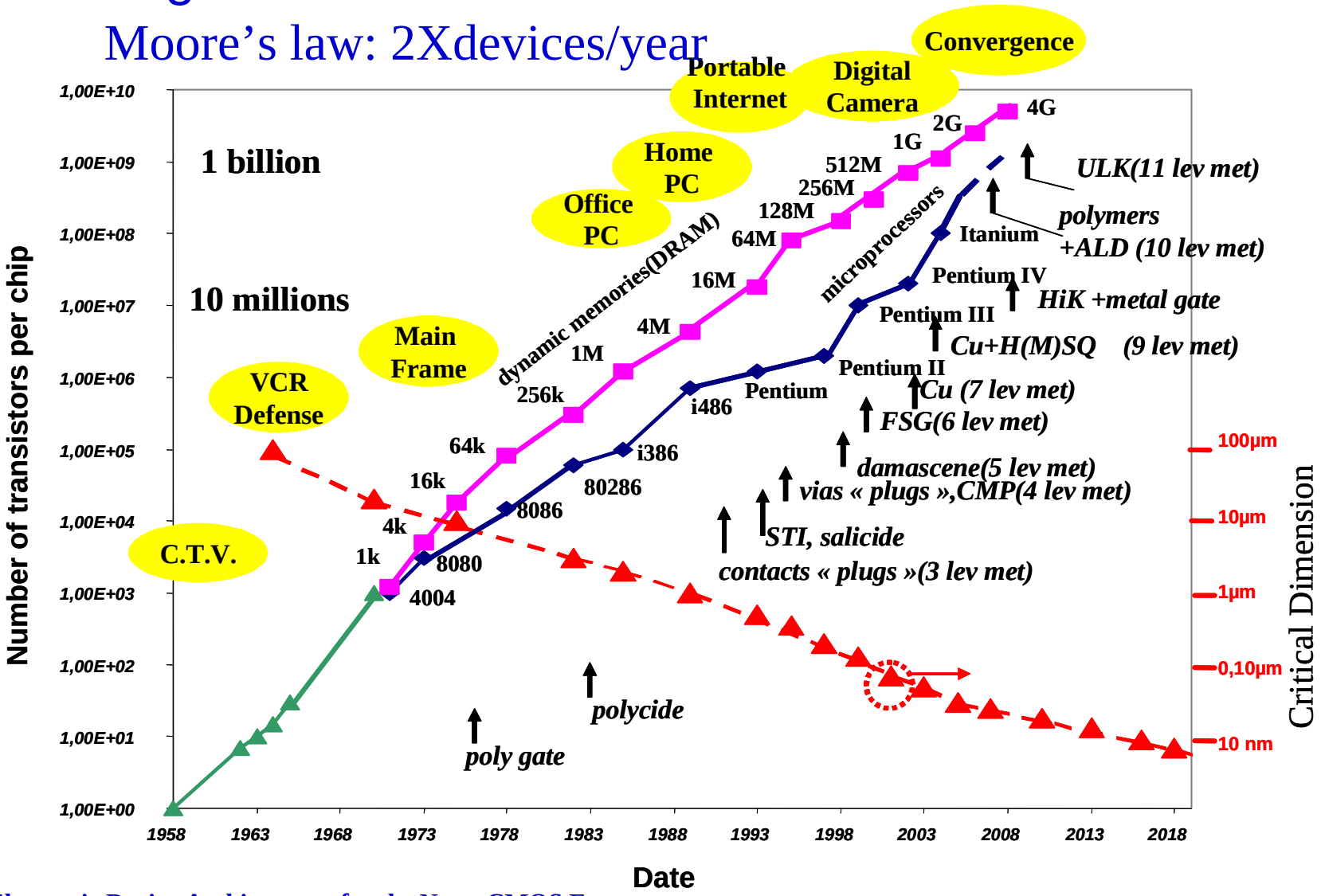
Semiconductor Market applications successive waves

Quality of life, Social, Environment, Health, Energy, …associated to ICT



Source : Semico Research Corp. May 2004 IPI Report

Scaling: a success story…thanks to innovation
Progress law for microelectronics
Moore's law: 2Xdevices/year



Electronic Device Architectures for the Nano-CMOS Era
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Editor: S.Deleonibus, Pan Stanford Publishing, Oct 2008

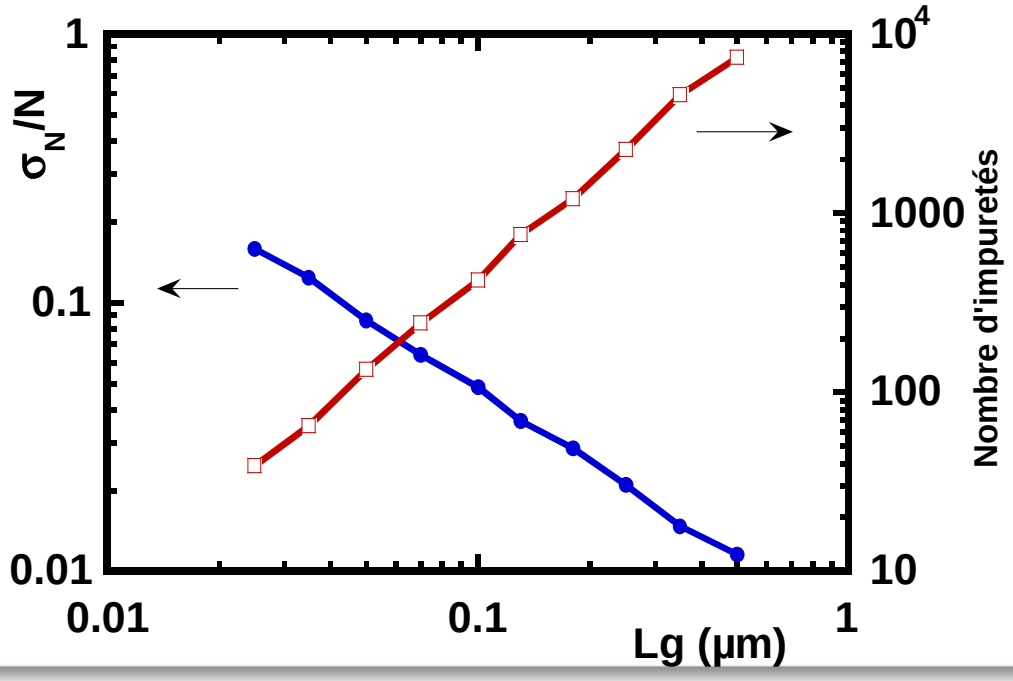
Hot Topics: parasitic effects in MOSFET technology

- Introduction of HiK and metal gate allows continued scaling and relaxes SiO2 gate leakage current related issues - Ig added to SCE, DIBL, subthreshold leakage(LETI IEDM 2002, Intel IEDM 2005)
- Statistical dopant variability

  - number of dopants in the active area decreases with scaling

  - random distribution of channel dopants

  Poisson's law. Standard deviation:



$$\sigma_{doping} = \left(\frac{N}{Volume} \right)^{1/2}$$

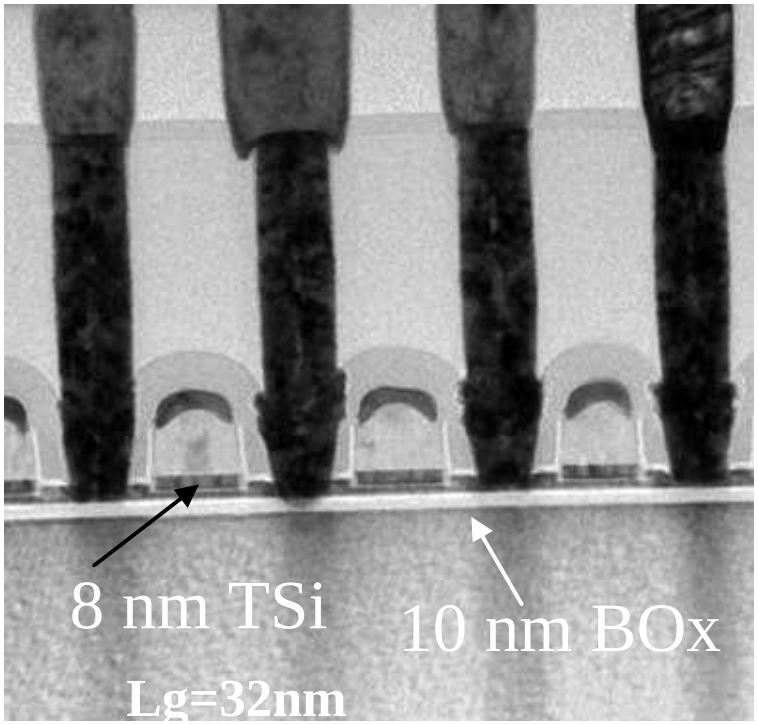
Statistical fluctuations of threshold voltage: 150 mV decay for VT=200mV(Lg=25nm) !!

Major interest for Low Doped channels

Low Power FDSOI Thin Films Undoped channels

300mm wafers

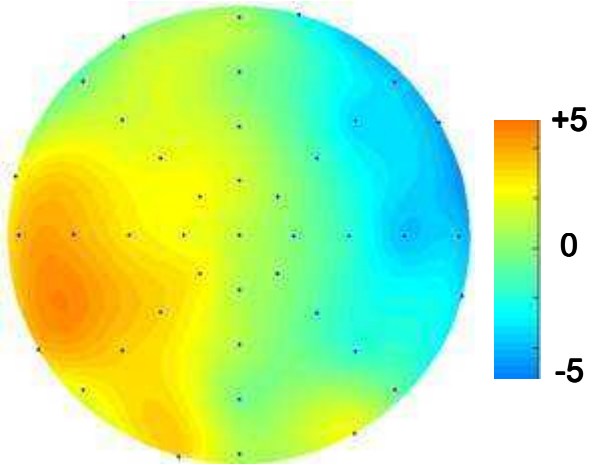
6T SRAM



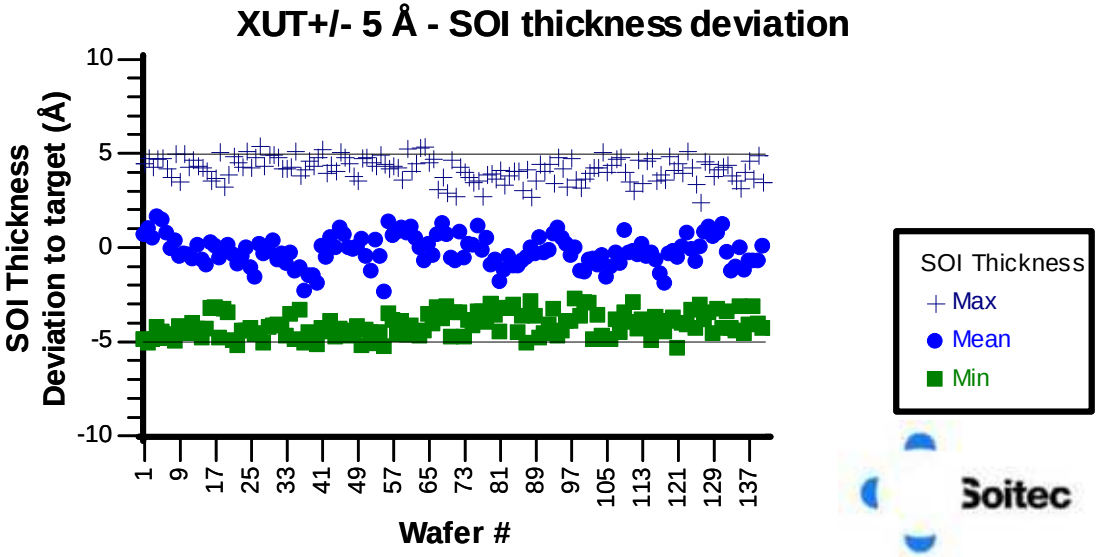
0.248µm² SNM (1.2V)=140mV

0.179µm² SNM (1.2V)=230mV

VDD=1V Ioff=6pA/µm



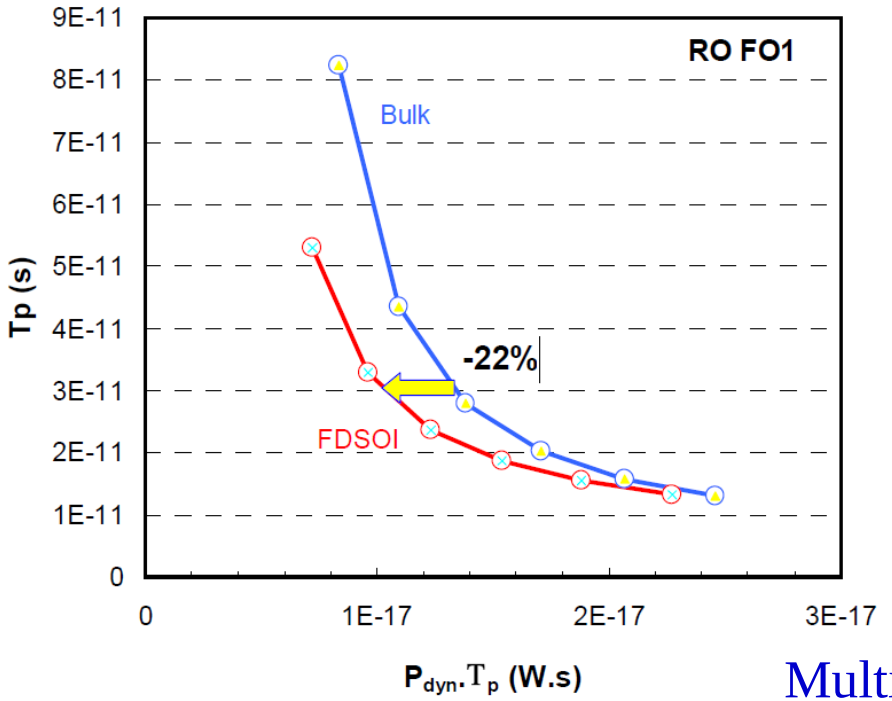
Range = ±4 Å!



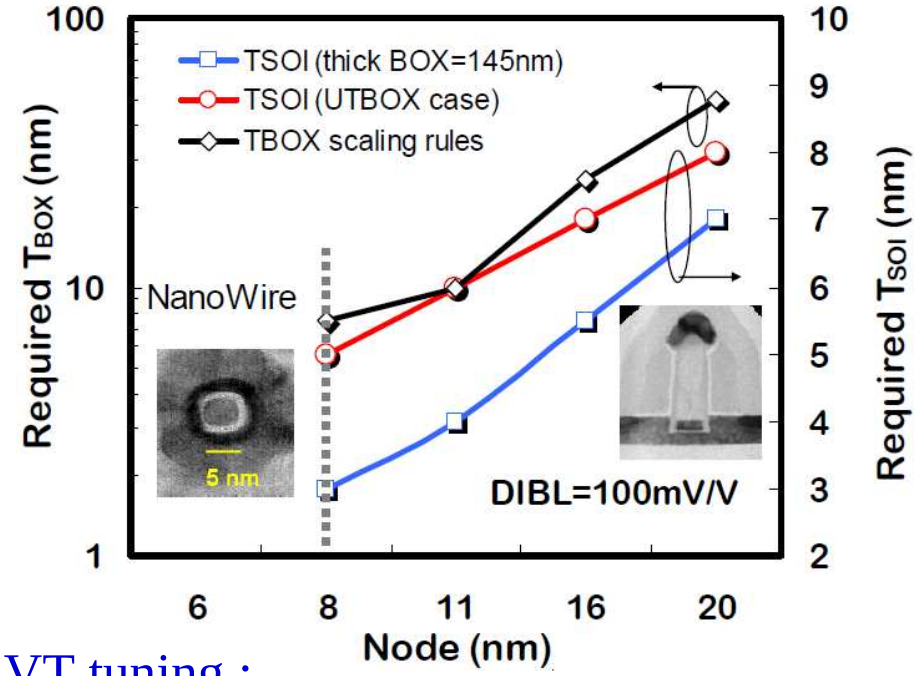
LETI, ST Micro: C.Fenouillet Beranger et al., IEDM 2007, VLSI Symp 2010
V.Barral et al., IEDM2007

Merits of FDSOI Thin Films Undoped channels

Delay vs. Power x Delay
22% improvement/bulk (20nm)



Reachable Scaling rules
(TSi, TBOx)



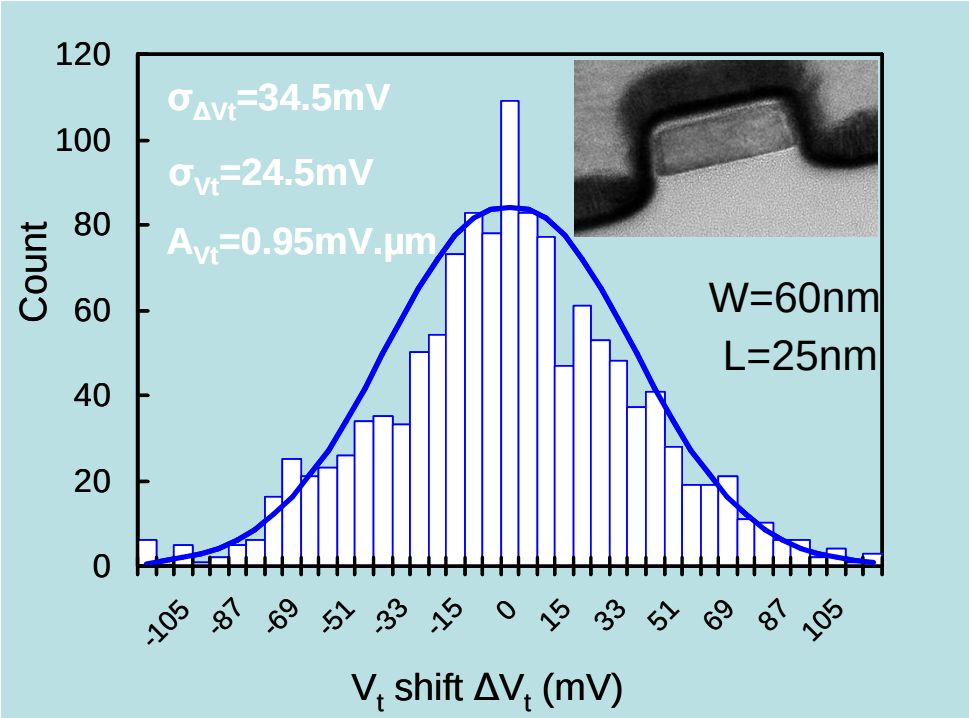
LETI, SOITEC, STMicro :
O.Faynot et al., IEDM 2010 , invited talk
L.Clavelier et al, IEDM 2010, invited talk
F.Andrieu et al. , VLSI 2010 Honolulu
L.Hutin et al., IEDM 2010
P.Nguyen et al , VLSI Tech 2011

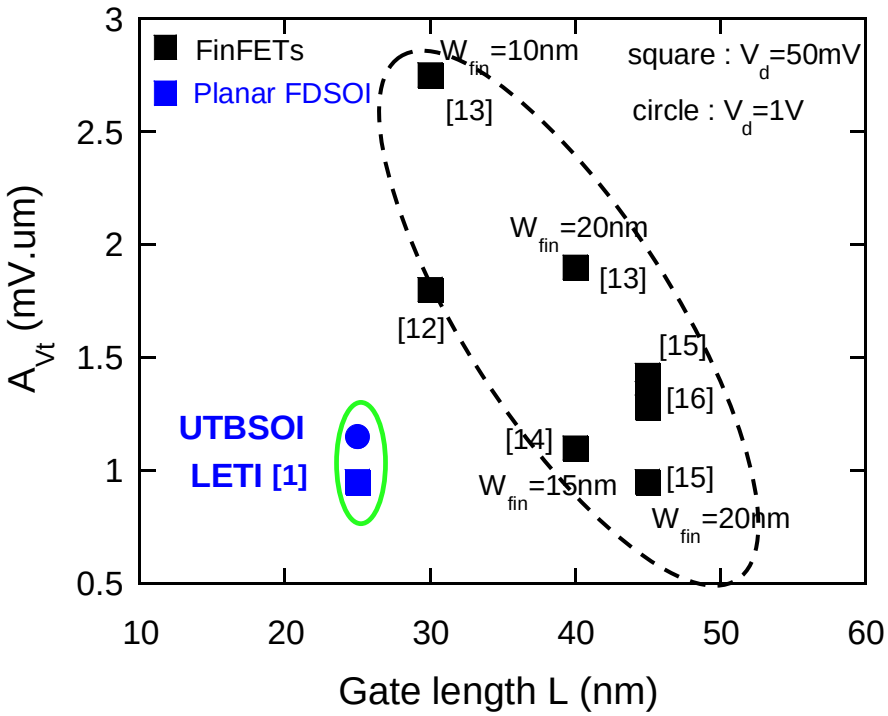
Multi VT tuning :

- BOx+ back bias ;
- Gate stack engineering;
- BOx engineering(ch.injection)
- Dual strained channels(40% improv. τ_p)

FDSOI Undoped channels vs.FinFET

Record-high V_T matching performance





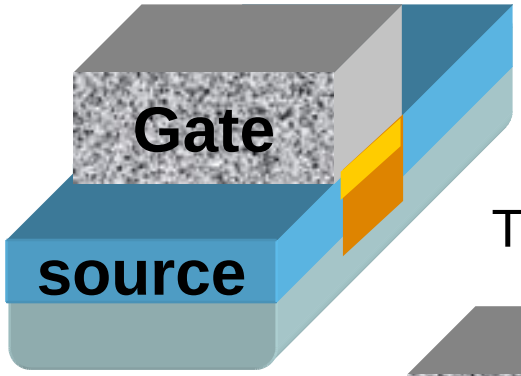
LETI: O.Weber et al., IEDM 2008

($\sigma_{Vt}=\sigma_{\Delta Vt}/\sqrt{2}$ to compare measurements on pairs and on arrays of transistors in the literature)

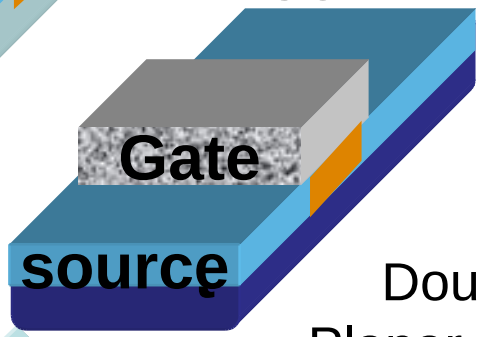
$$\sigma_{Vt} = \frac{A_{Vt}}{\sqrt{WL}}$$

Best trade-off between V_T variations and gate length scaling compared to bulk MOSFETs and FinFETs

Bulk or thick SOI

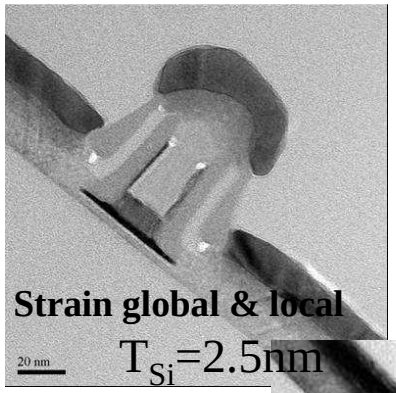


ThinSOI



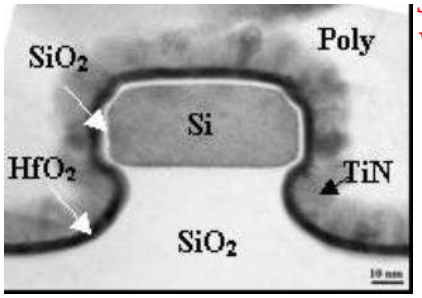
Planar

T_{Si}= ¼ Lg

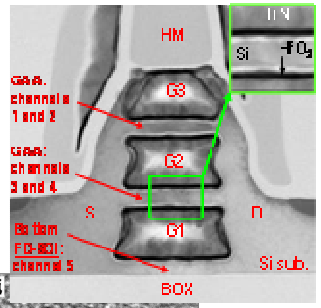


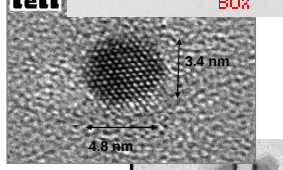
Barral et al. IEDM2007

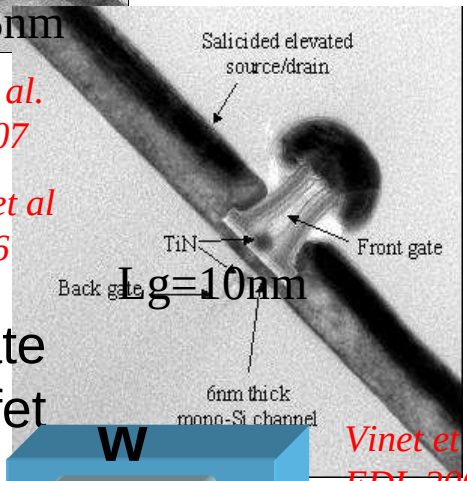
Andrieu et al VLSI2006



Jahan et al. VLSI2005

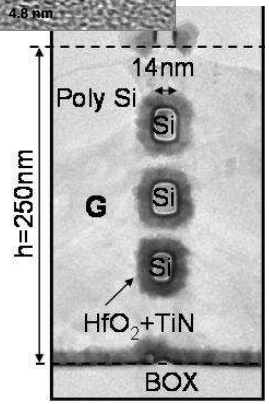


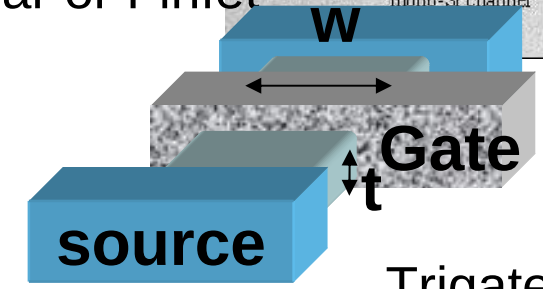




Double-gate Planar or Finfet

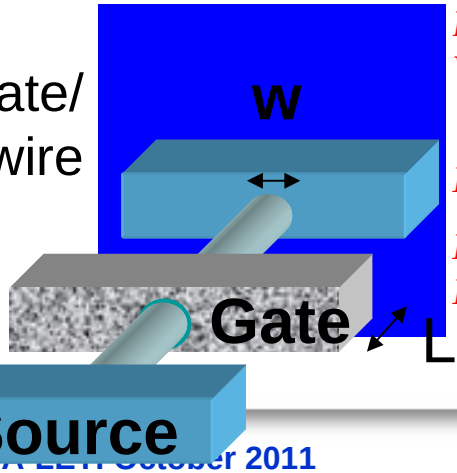
Vinet et al. EDL 2005





T_{Si}= ½ Lg

Trigate/ nanowire



Bernard et al VLSI 2008

Dupré et al. IEDM 2008

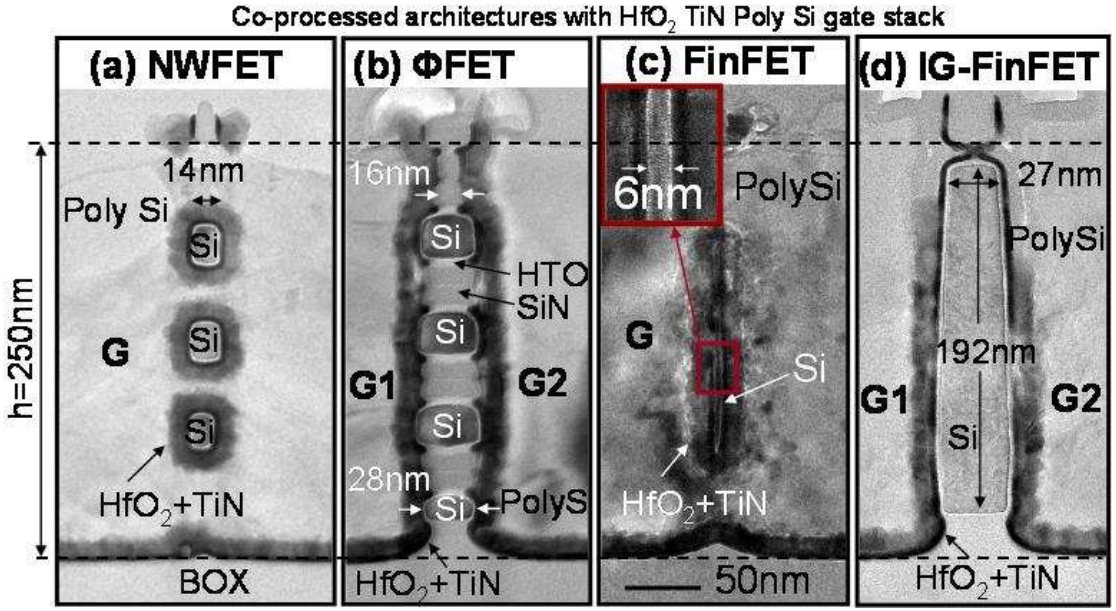
Ernst et al. IEDM 2008

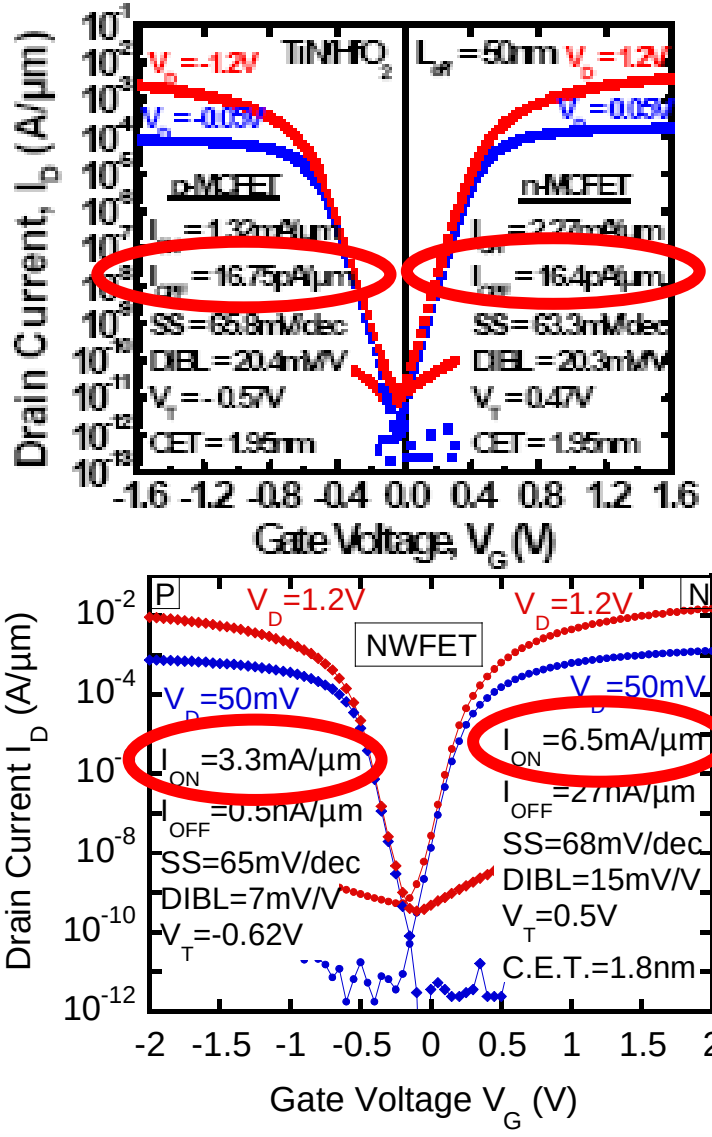
T_{Si}= 1 to 2 Lg

Thin Films Devices

Relaxing optimization scaling rule by architecture

Stacked Multichannels and MultiNanowires « Top-Down » approach





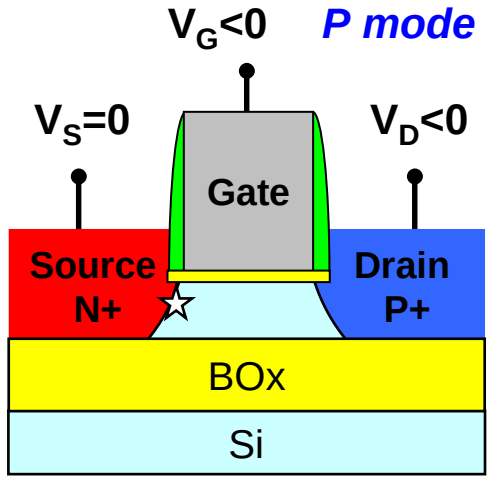
LETI top down approach for Low Power and High performance

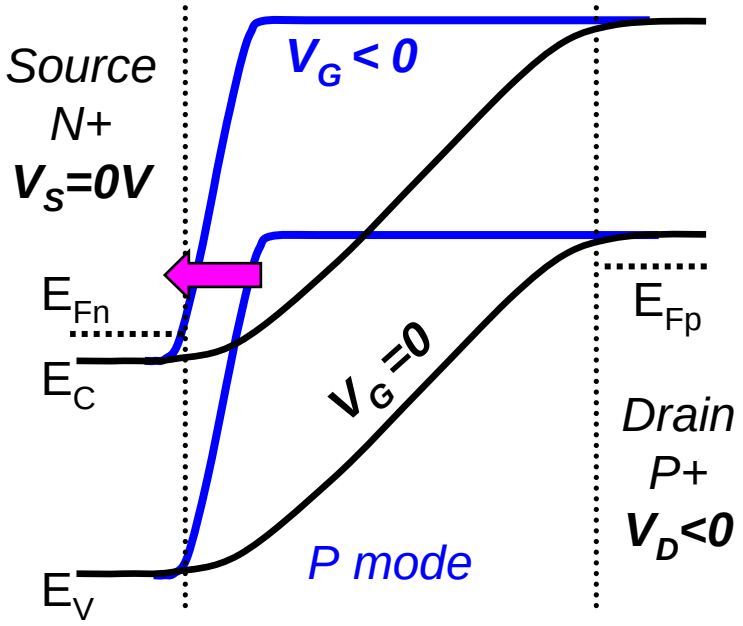
- -CV/I outperforms Planar in loaded environment
- -Gate separation possible
- -Transport properties in small nanowires
- -Flexibility to tune channel conductance wrt FinFET
- -Pervasion into microsystems (More than Moore)

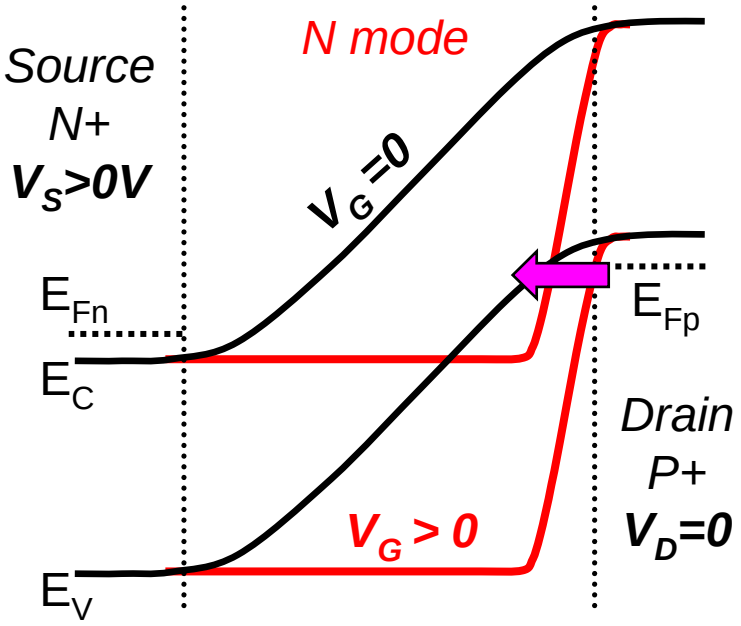
LETI: Dupré et al. IEDM 2008, San Francisco(CA)
Ernst et al., Invited talk IEDM 2008, San Francisco(CA)
Bernard et al, VLSI Symposium 2008 Honolulu
K.Tachi et al., IEDM 2010, San Francisco

Tunnel FET Operation principle

- N & P operation modes
  - A single TFET device can operate either in n or p channel mode
    - N mode : $V_{SD}>0$ & $V_{GD}>0$
    - P mode: $V_{DS}<0$ & $V_{GS}<0$

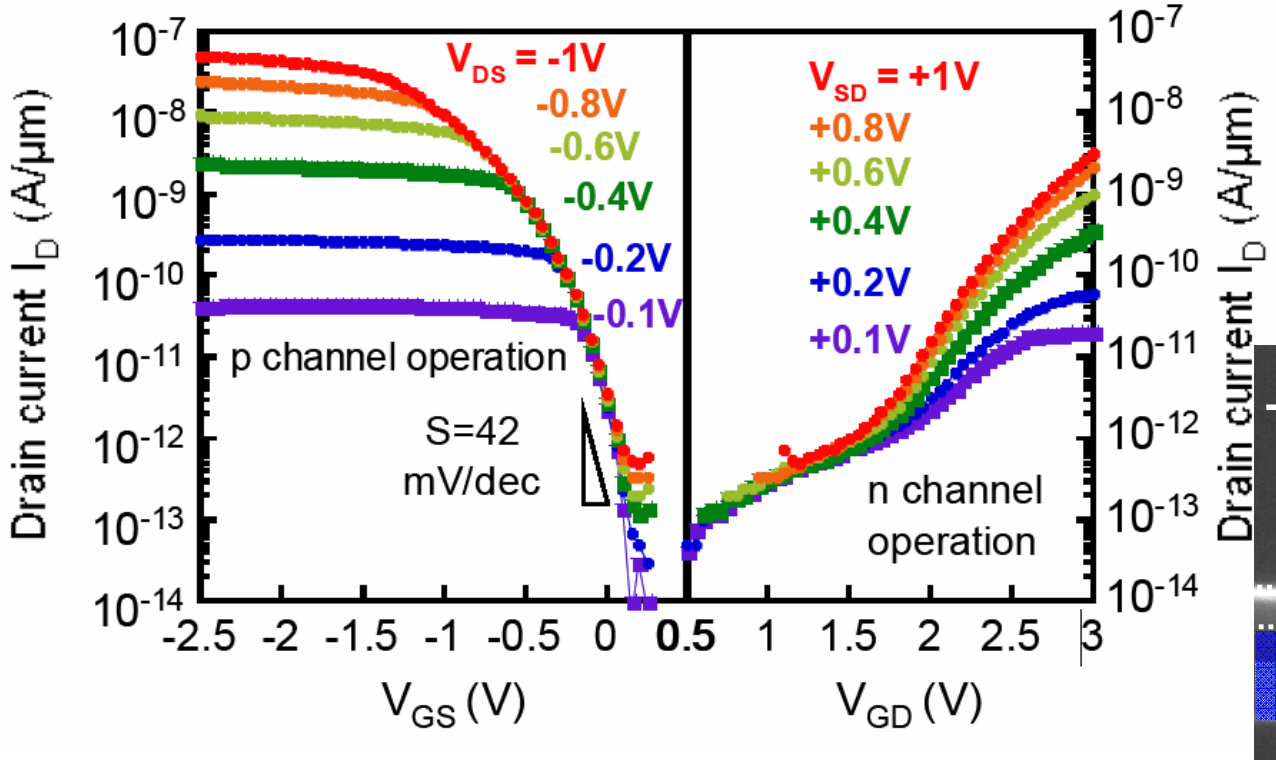


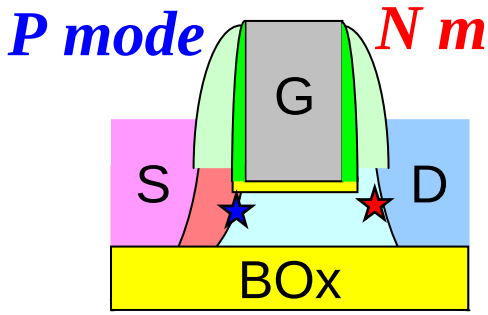




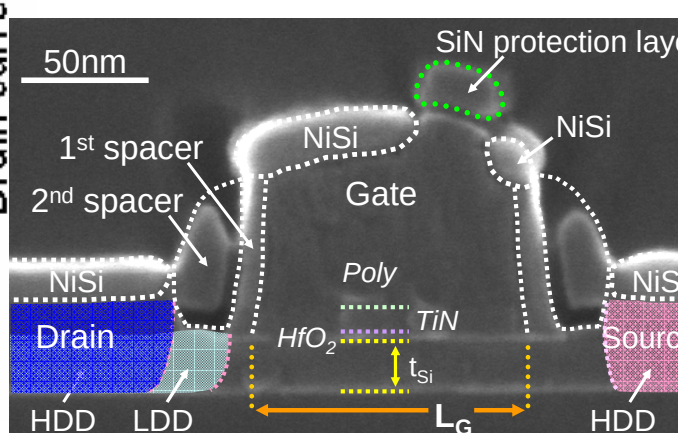
SOI TFETs co-integrated with CMOSFETs

Experimental demonstration
of Tunnel FET operations:





SOI TFET
w. LDDn



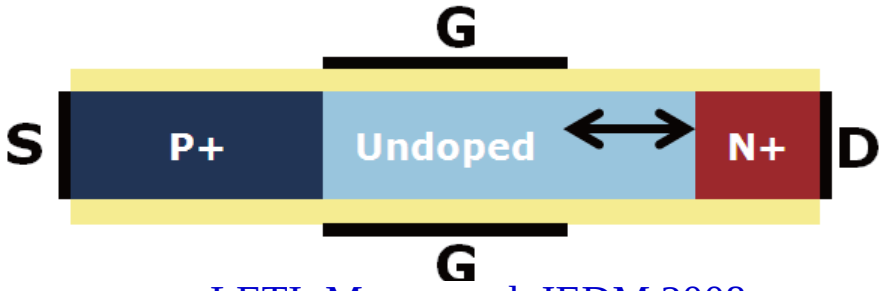
•P mode: V_{DS}<0 & V_{GS}<0

L=100nm; T=300K

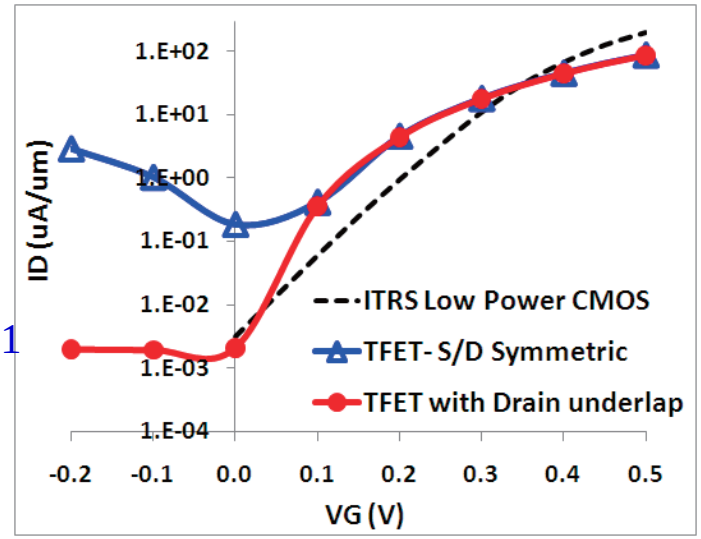
•N mode: V_{SD}>0 & V_{GD}>0

F.Mayer et al., IEDM 2008,
C.LeRoyer et al., ULIS 2009

TFET for Ultra Low Power outperforms CMOS
Offset/drain reduces Ioff(ambipolar current)

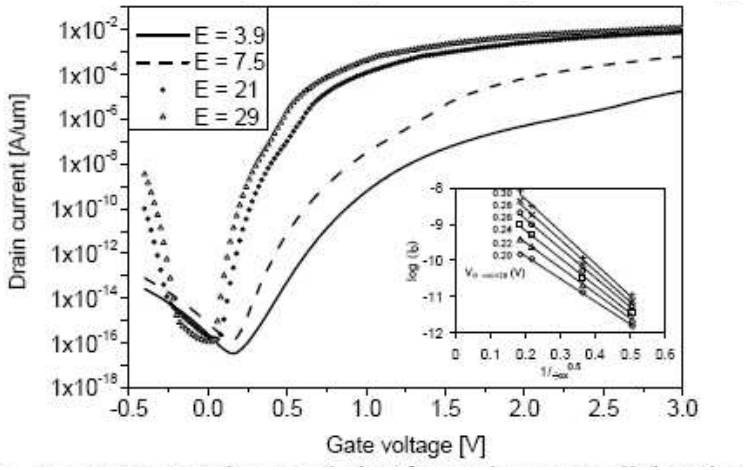


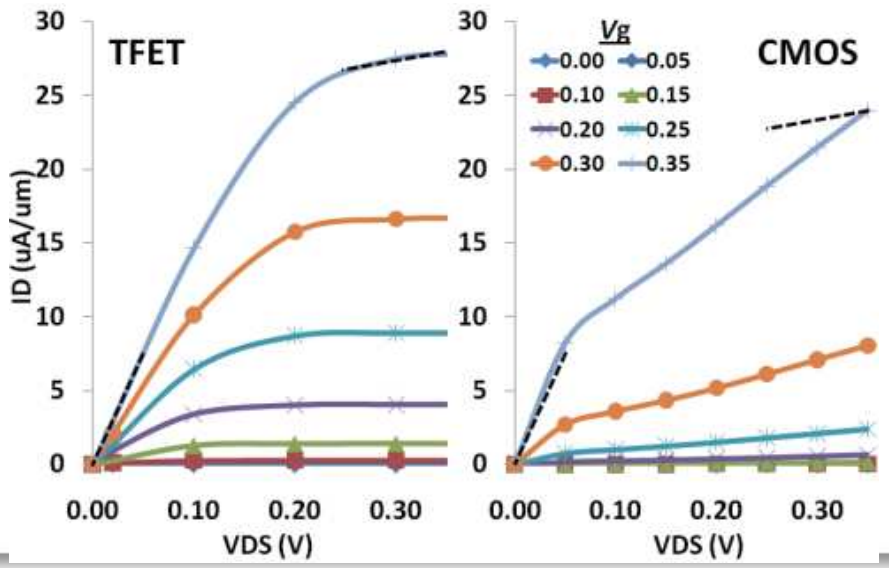
LETI: Mayer et al, IEDM 2008
Intel: U.E. Avci et al, VLSI Tech Symp 2011



Multigate improves Ion

EPFL: K. Boucart & A. M. Ionescu, ESSDERC 2006
TUM: M. Schlosser et al. IEEE TED, Jan. 2009





Opportunities for other materials on Silicon

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Material	μ_n ($cm^2V^{-1}s^{-1}$)	μ_p ($cm^2V^{-1}s^{-1}$)	s_{th} (W/m/K)	Rel. K	Eg(eV)	v_{sat}(10^7cm/s)	ni(cm^{-3}) $(m^*_e m^*_h/m^2)T^{3/2}$ exp(-Eg/2kT)
Si	1400	500	141	11.9	1.12	0,86	$2x10^{10}$
Ge	3900	1900	59.9	16	0.66	0,60	$2x10^{13}$
GaAs	8500	400	55	12.9	1.42	0.72	$2.1x10^{6}$
$InGa_{0.47}As_{0.53}$	12 000	300	5	13.9	0.74	0.6	$6X10^{11}$
InSb	77000	850	1.8	16.9	0.17	5.0 @77K	$2x10^{16}$
C-Diamond sp3	2200	1800	2000	5.7	5.47	2,7	10^{-27}
Graphene (CNT) sp2	10^4-10^5	10^4-10^5	1000	5.7	Semi-metal	4	$1x10^{12}cm^{-2}$ ($1x10^{15}$)

Well established high quality material (>40yrs experience) **Oxidizable !**

Silicon compatible
Available in all fabs
GaAs lattice constant matching

Opto/Power RF applications
Ge compatible
HP N channel

BTBT TFET/vW

Poor short channel effect immunity

Highest μ_n but Worst μ_n/μ_p!!

Passive layer combine w BOx (thermal shunt)

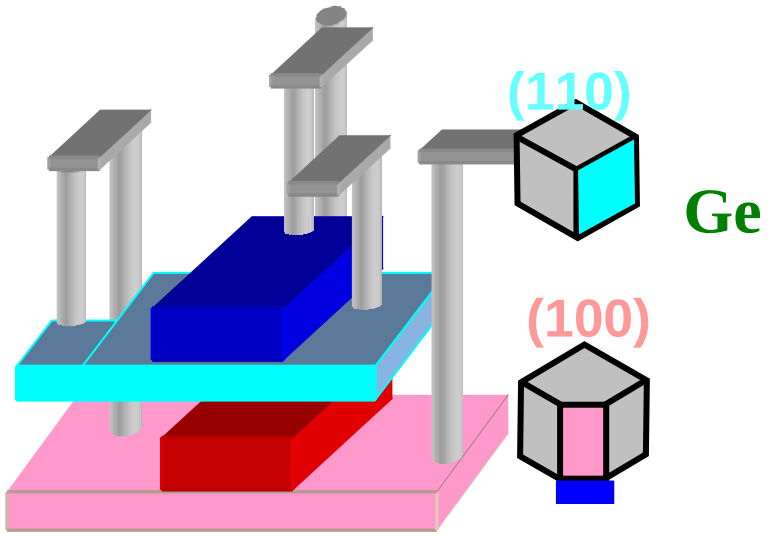
Highest σ_{th}

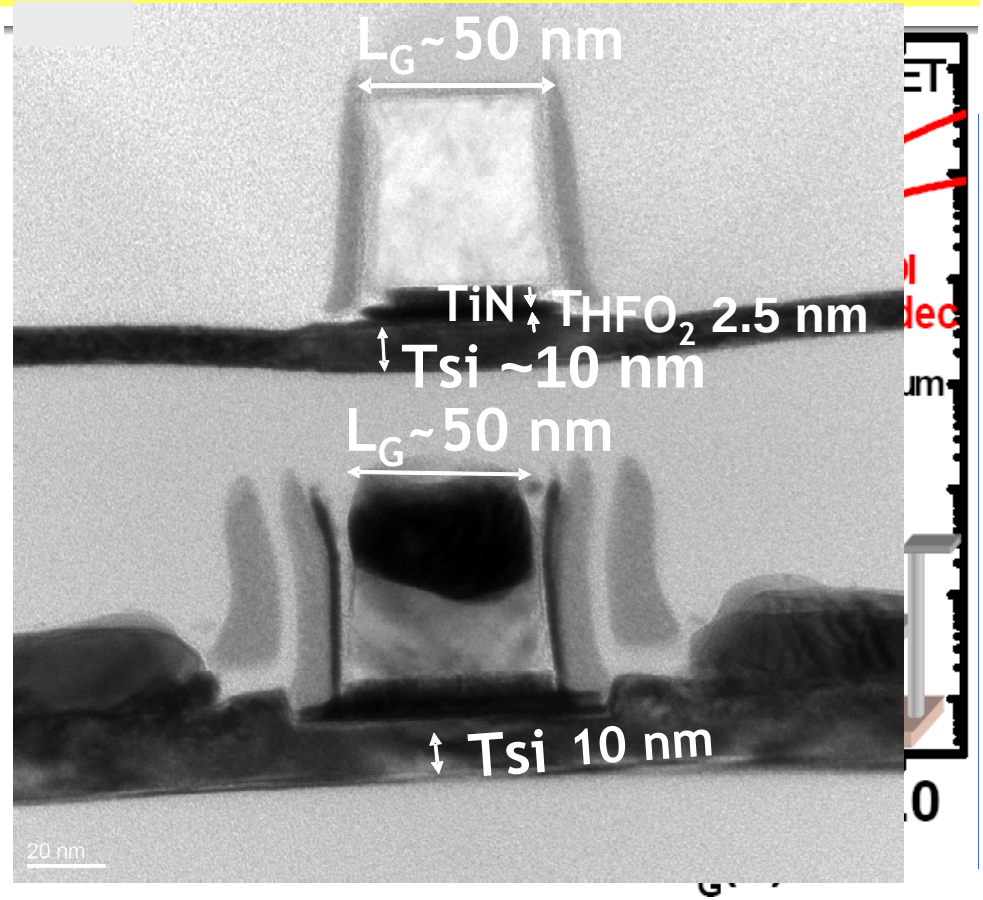
High short channel effect immunity

Most compact logic, Interconnect

3D sequential process

Co-Integrating Heterogeneous orientation or materials





- cold end process(bonding) Improved Ig

Opportunities for other SC(Ge,III-V, C, ...)

- improved layout (40% area SRAM cell)
- 4T SRAM
- dynamically controlled VT:

improved RNM and SNM

P.Batude et al., Best student Paper Award, IEDM 2009

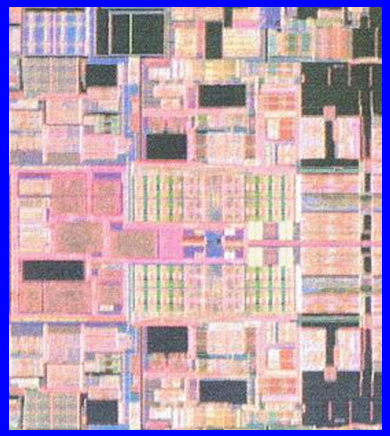
P.Batude et al, 2011 VLSI Tech Symp

First heterogeneous orientation in 3D Si sequential integration

Enabled by use of wafer bonding by keeping low thermal budget

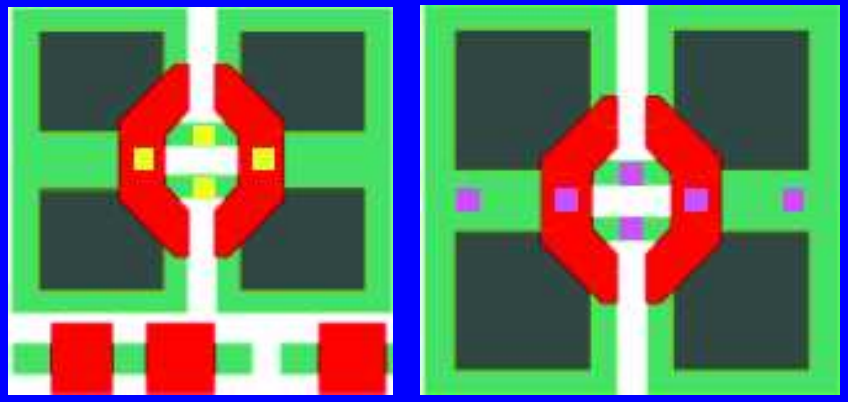
Sequential 3D: Potential and Demonstrated Applications

High density logic applications



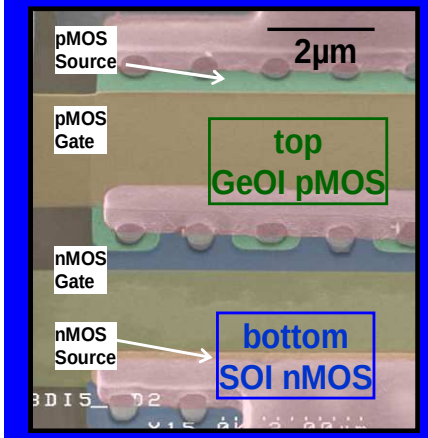
~ 1 node gain with same design rules for Front end levels

Highly miniaturized CMOS imagers pixels



P. Coudrain et al, IEDM 08,

Heterogeneous integration

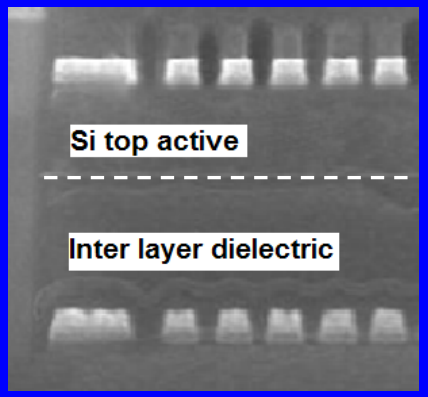


- Nanoelectronics & Photonics applications with Si-Ge Co-integration
- SRAM on top SOI logic, I/Os, analog on bottom bulk
- …

P. Batude et al,VLSI09

3D memories

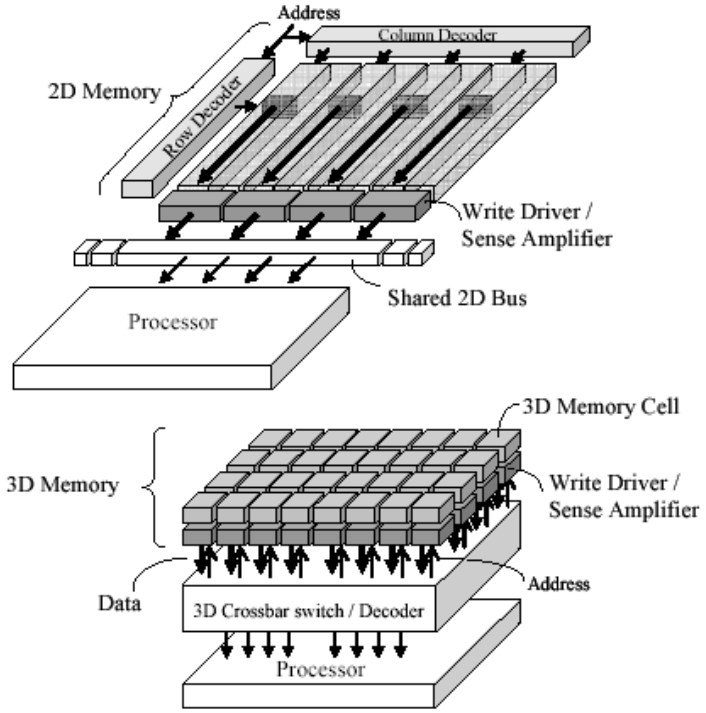
- SRAMs
- FLASH

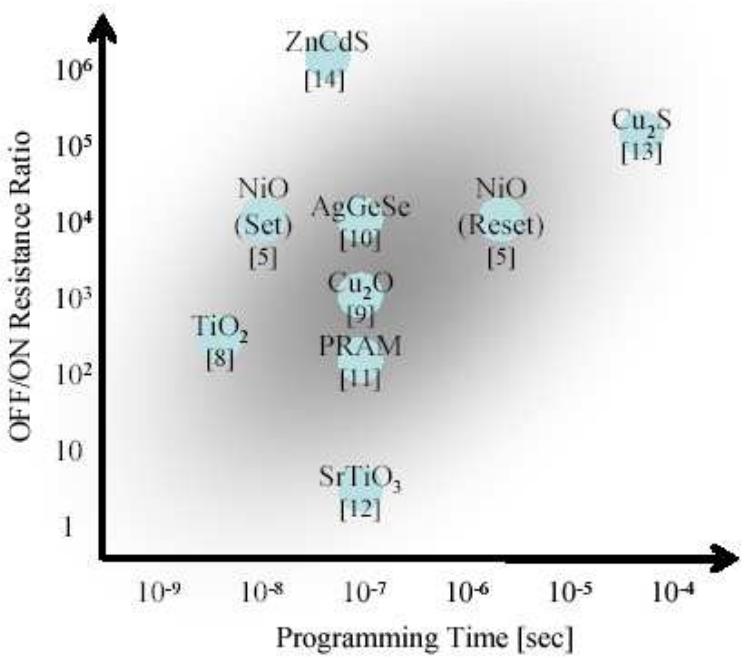


Y-H. Son et al, VLSI 07, Jung et al, IEDM 2006

P.Batude et al., IEDM 2009, Best Student Paper Award

3D-Xbar Memory stacked on Logic: towards NV Logic





Resistive switches

Toshiba, Stanford Univ.: K.Abe et al, ICICDT 2008

Logic + Stacked NVM:

High bandwith,

Reduced Power consumption,…

Reconfigurability

ex: 32 nm node : > 1TB/s per $1mm^2$

proven in 2D with

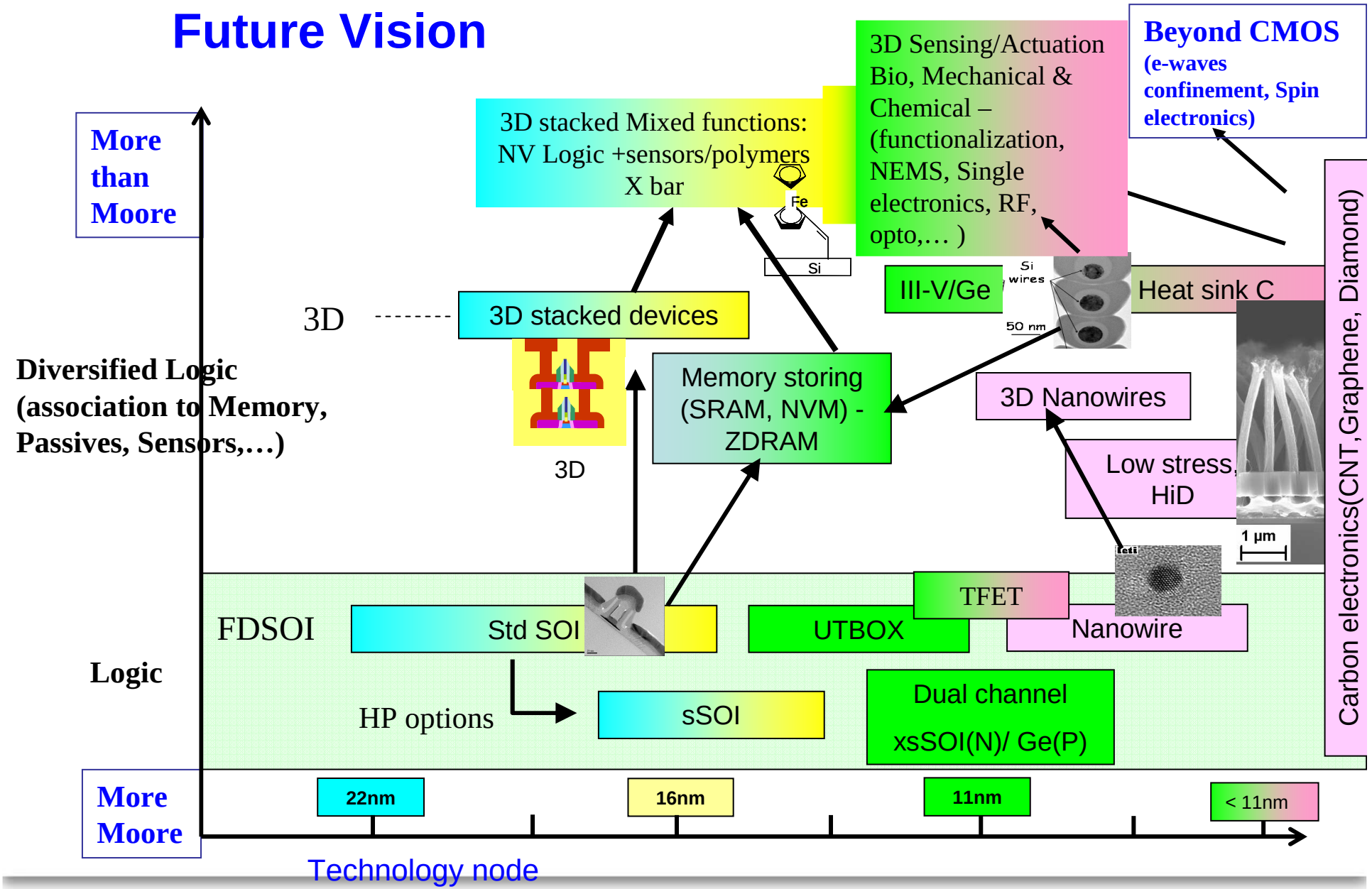
Magnetic Tunnel Junctions,

FeRAM ***Tohoku Univ., Hitachi:***

S.Matsunaga et al., Appl.Phys. Express(2008);

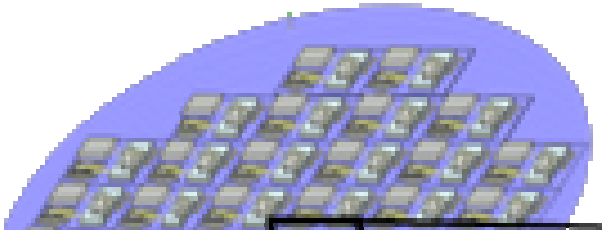
ROHM

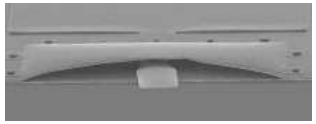
Advanced Devices and Systems Future Vision

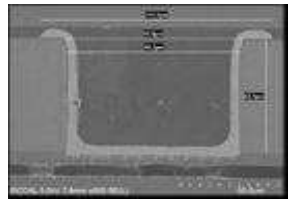


System On Wafer: Heterogeneous co-Integrated Systems

(Parallel 3D)



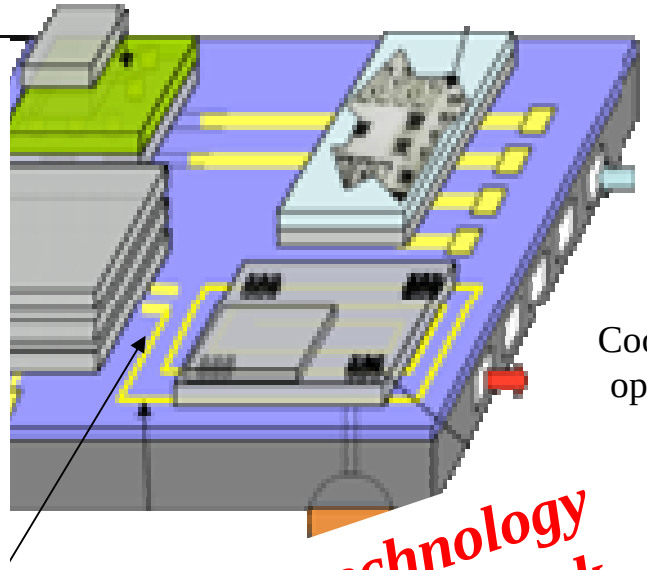




Energy source converter

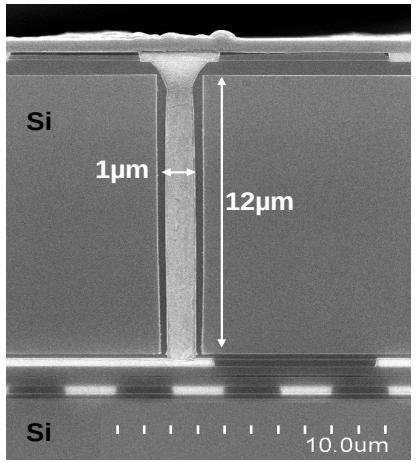
Wafer level packaged MEMS

MEMS



Cooling option

80 µm diameter TSV imagers packaging



1 µm diameter
High AR TSV stacked ICs

Commercial products

- image on board VGA camera,
- mixed nodes & modes,
- high density TSV

Cross talks:

-delay, matching,

-power dissipation
(global temp. increase,
hot spots, reliability, …)

Multiphysics

New Progress Laws

- application specific

Via belt technology
MEMS + IC stack
Ultra flat 3D
Chip stacking(TSV)
Active Silicon interposer

'Cs

On Silicon

account

wafer level

3D Integration: from imagers to advanced 3D ICs

ST – LETI collaboration

2001

2008

with TSV

VGA cameras (300kpixels)

Image-on-Board

Mixed Signal Digital/Analog

170µm
30µm
120µm
80µm
400µm

Pitch 120µm
Pitch 50µm

ST – LETI collaboration

ØTSV~3µm
Thin Si~15µm
ØTSV~3µm
Thin Si~15µm
Metal1

3D-IC

Memory, Processors, Imagers with high density TSV, NEMS…

Thinned wafer (~100 µm)

Die to Die Copper pillars

Diam 60µm
Thick 120 µm

Via Last TSV (Aspect Ratio 2-3)

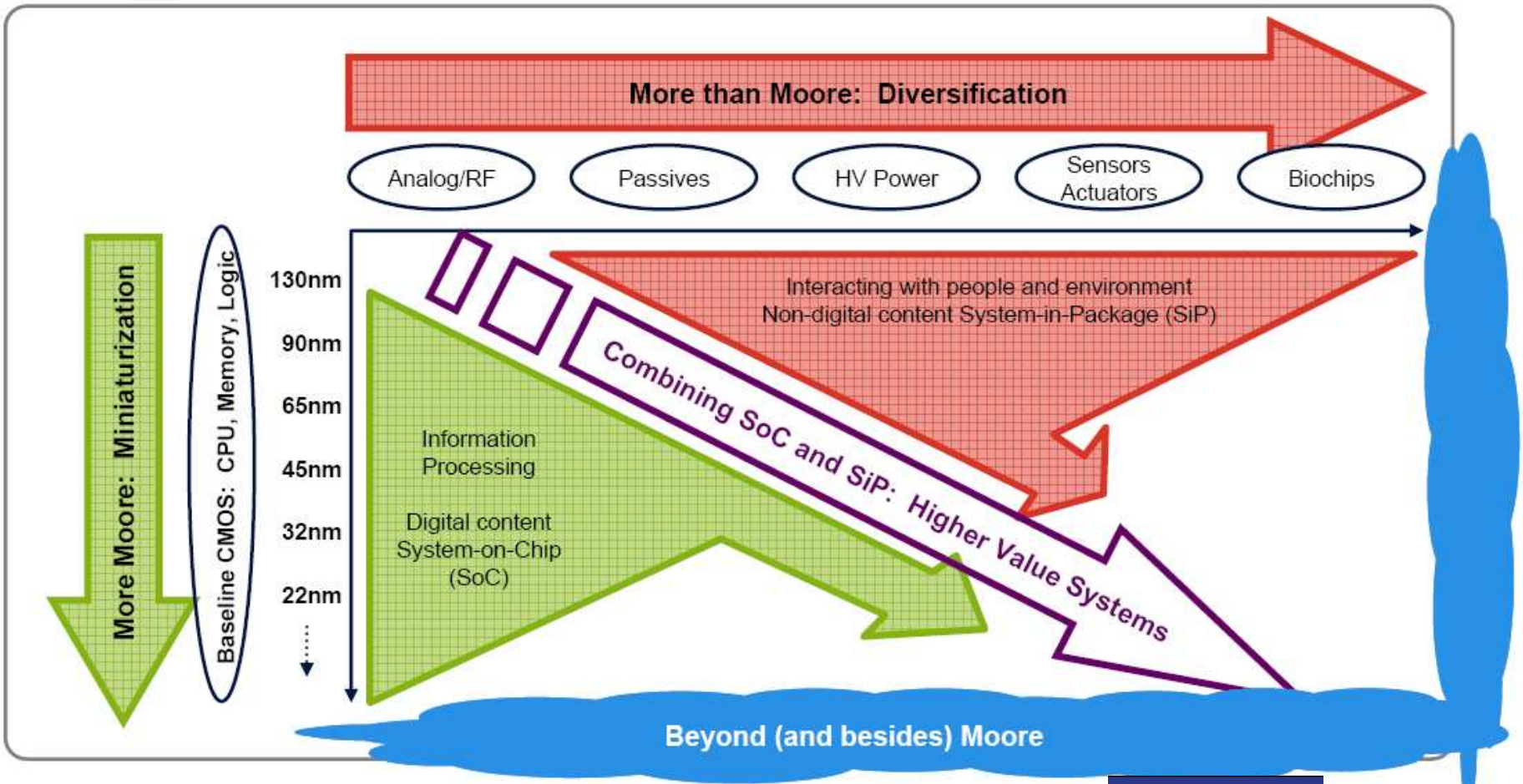
Die to substrate copper pillars

Active Silicon interposer

3D high density

« More, More than, Beyond Moore »

Tomorrow's top added value markets



High growth with 'More than Moore' technologies:
they require **expertise** in all technical domains and in-depth knowledge of the targeted markets ***ITRS 2009***

NEMS scaling laws: is it worth?

- resolution increases
- sensitivity decreases (SBR,SNR) => arrays, actuation,…
- figures of merit pressure and vacuum quality dependent

$$\delta m = \frac{M_{eff}}{Q} \cdot 10^{-(DR/20)}$$

$$DR \propto \sqrt{\frac{\sum S_{noise}}{P_{act}}} = \frac{1}{SNR}$$

ML Roukes et. al. APL (2005)

Parameter	Scaling rule
mass	k^3
stiffness	k
resonant frequency	k^{-1}
mass responsivity	k^{-4}
energy consumption	k^3 [rough estimate]

$$M_{eff} \propto l \cdot w \cdot t$$

$$\kappa_{eff} \propto w \cdot \frac{t^3}{l^3}$$

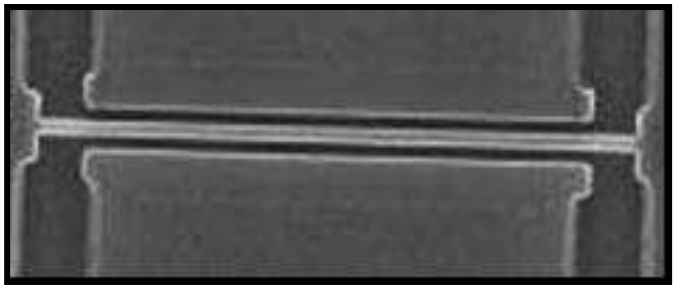
$$f_0 \propto \sqrt{\frac{\kappa_{eff}}{M_{eff}}} \propto \frac{t}{l^2}$$

$$\Re = \frac{\partial f_0}{\partial M_{eff}} = -\frac{f_0}{2M_{eff}}$$

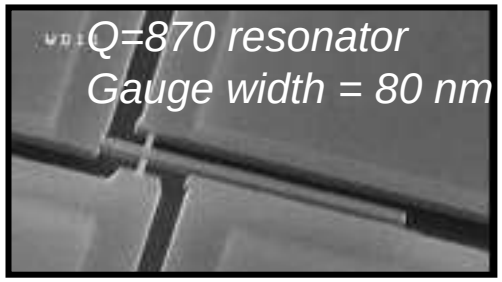
$$E_P \approx \frac{1}{2}\kappa_{eff} \cdot x_{Max}^2$$

and $x_{Max} \propto t$

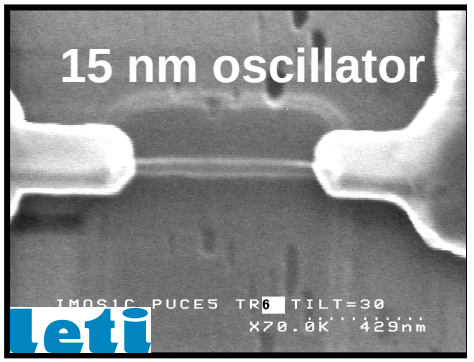
Nanowires & Arrays used for mass detection



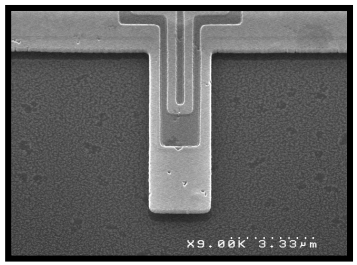
Capacitive actuation & detection



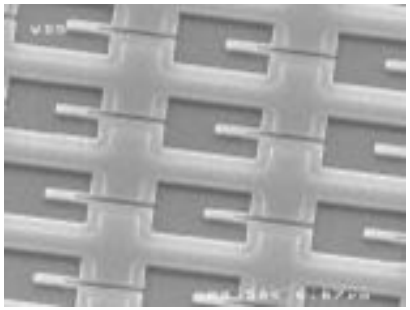
Capacitive actuation & piezo-resistive detection with nanowires



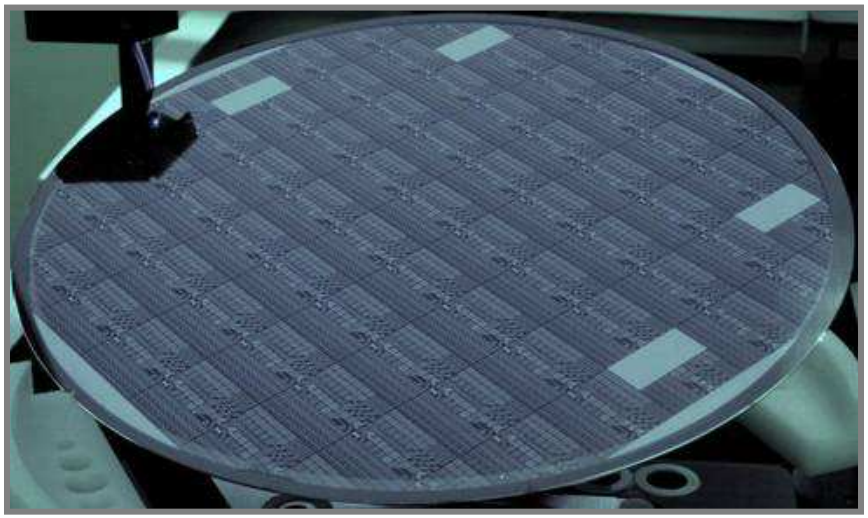
$$\delta m \approx 0.5\ zg/\sqrt{Hz}$$



Thermo-elastic actuation & piezo-resistive detection.



NEMS array



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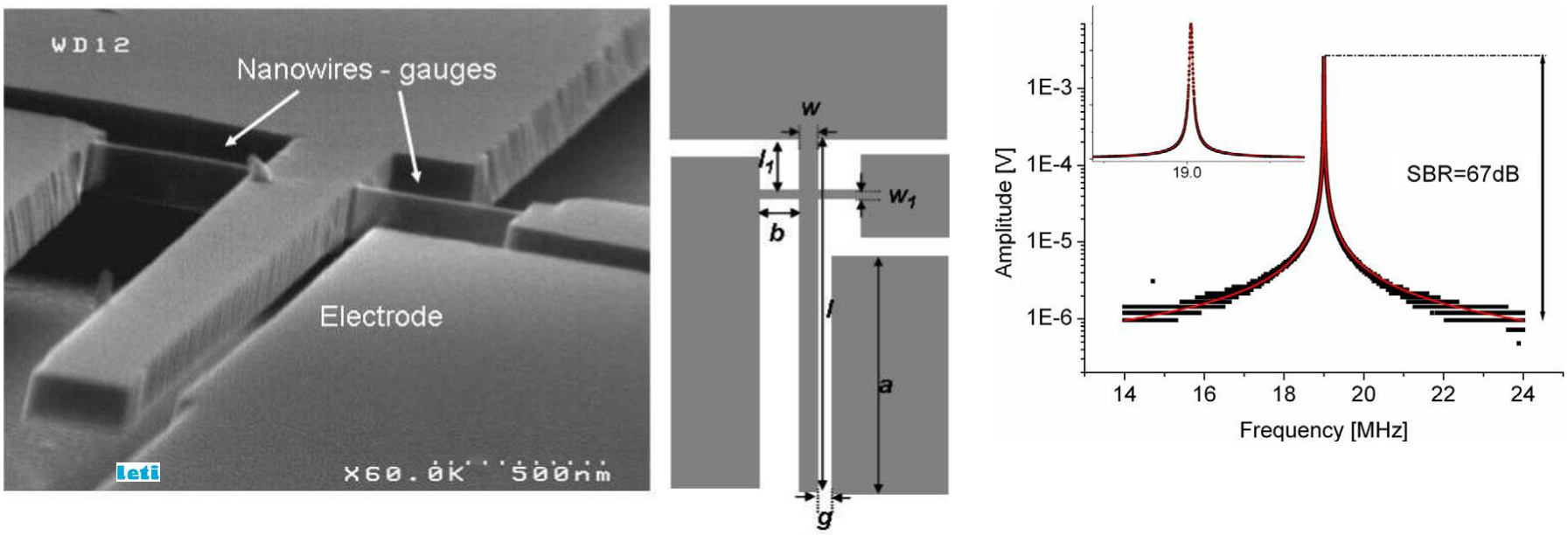
- First 200 mm wafers with 3.5 millions NEMS

- Association Nanowire/Resonator ; Cantilever arrays CMOS compatible

LETI: T.Ernst et al., IEDM 2008, Invited talk
L. Duraffourg et. al, APL 92, 174106 (2008)
E Mille et al, Nanotechnology, 165504, (2010)

A new design example

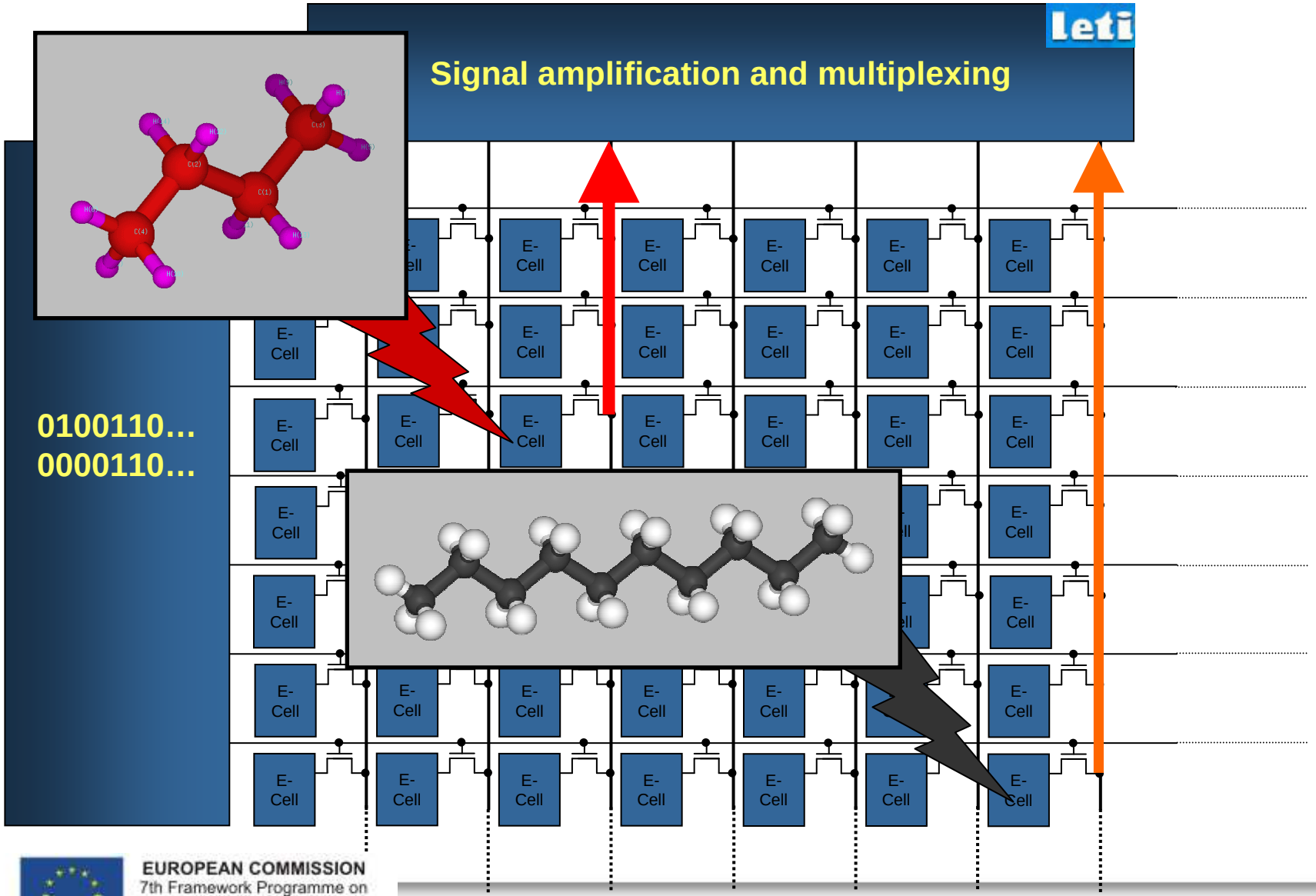


Electrostatic actuation

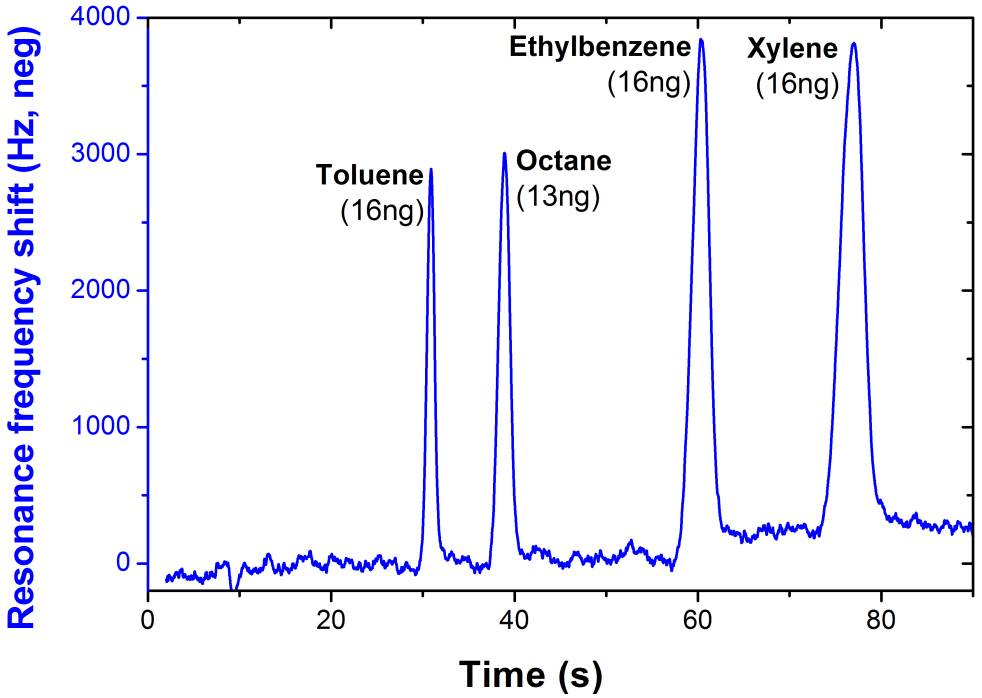
- **Piezzo resistive detection (down mixing scheme)**
- **Excellent Signal to background ratio**

E. Mile et al., Nanotechnology 21 (2010) 165504

A multi-physics system vision



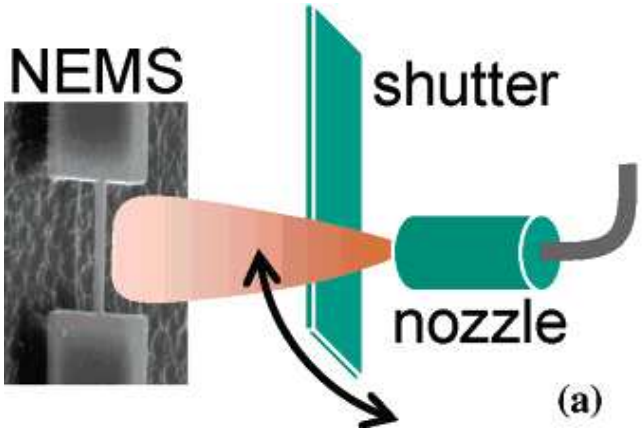
Gaz recognition

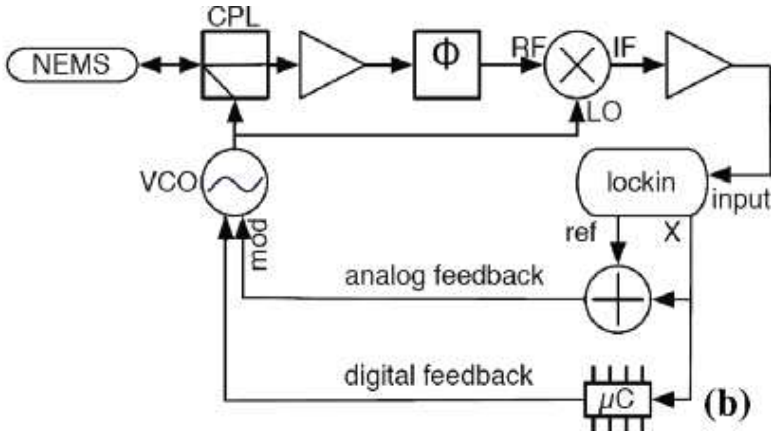


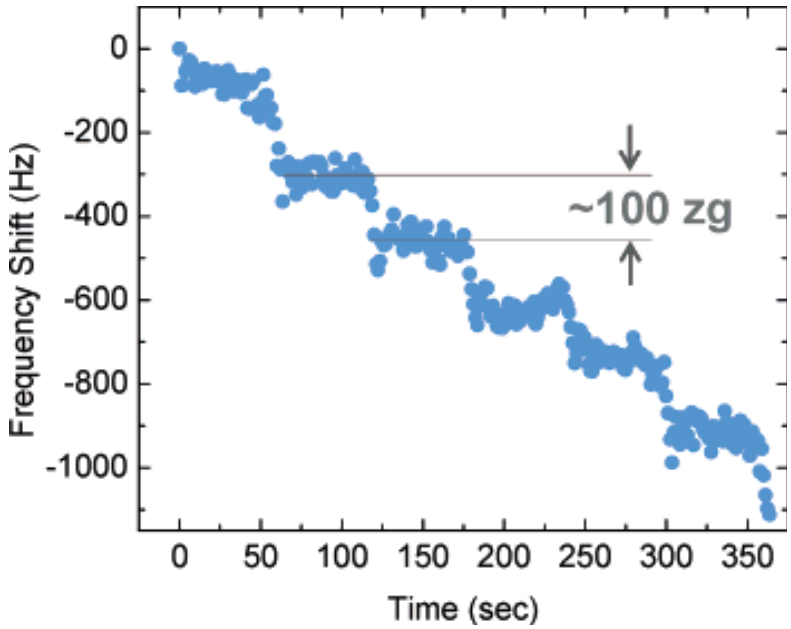
Partnership:

Apix, startup from
LETI and Caltech

Mass sensing demonstration





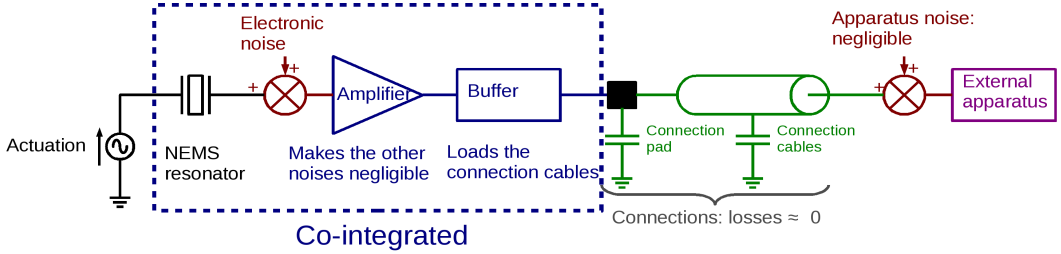


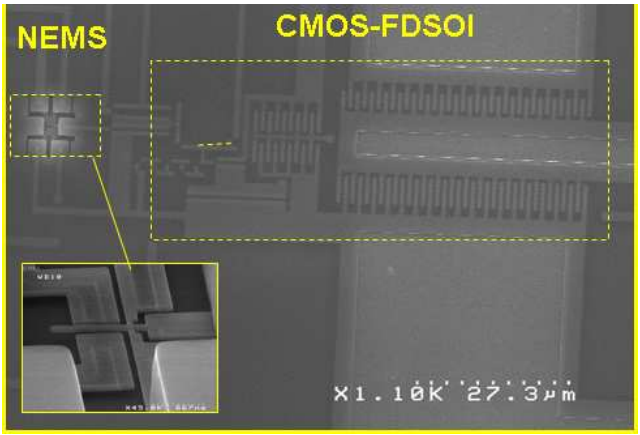
best mass resolution corresponds to 7 zg (30 xenon atoms)

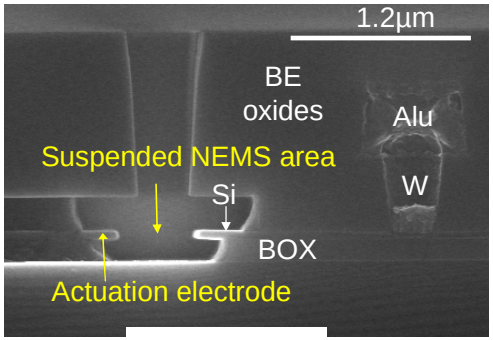
Yang et al., Nano Lett., Vol. 6, No. 4, **2006**

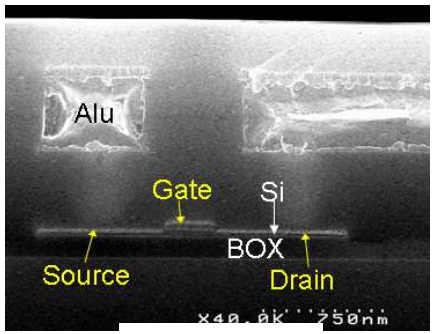
Front-end co-integration of ultra-scaled Si NEMS with FDSOI CMOS

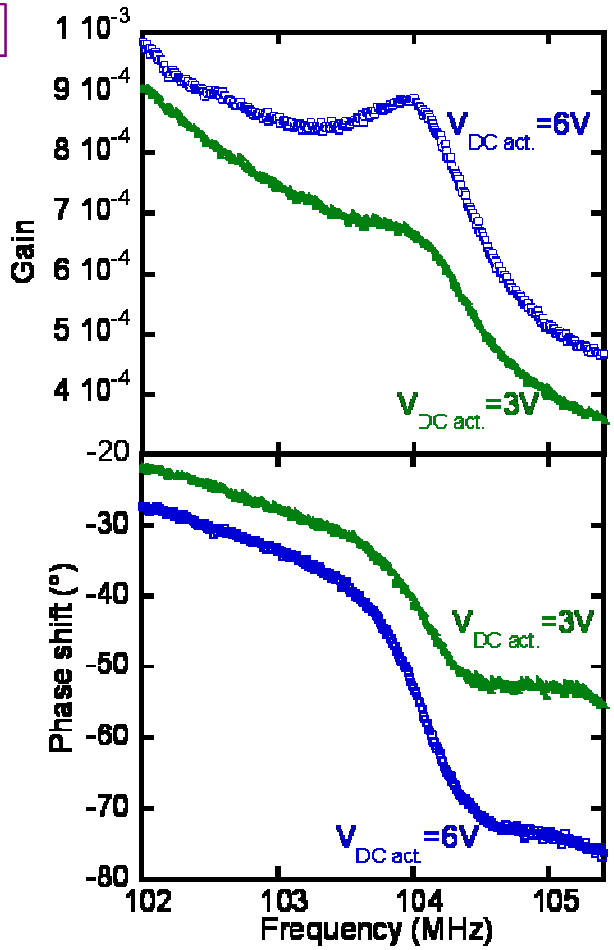
Integration of first amplification stage enables direct measurement of small electrical signals provided by the NEMS resonators (40nmx40nm cross section)





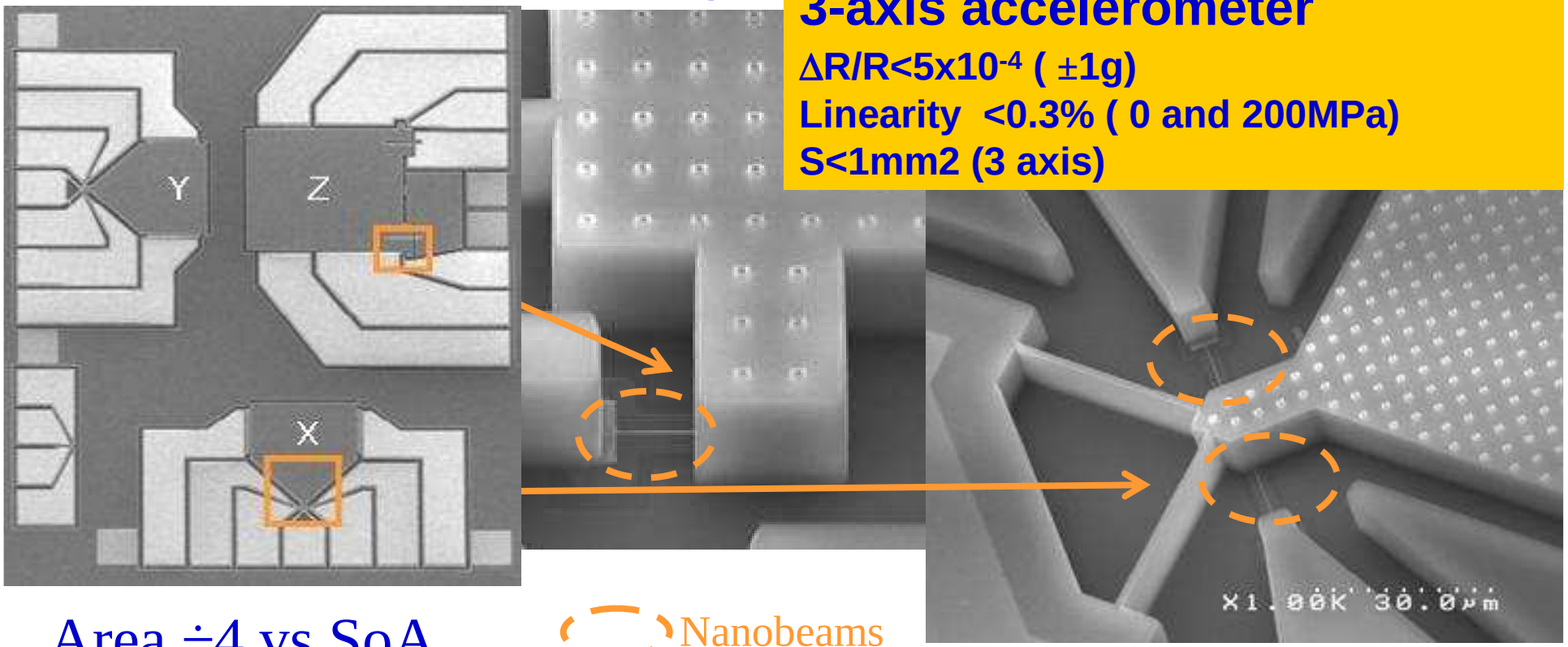






NEMS part ***CMOS part***

M&NEMS co integrated devices platform for 3D sensing



3-axis accelerometer

ΔR/R<5x10^{-4} (±1g)
Linearity <0.3% (0 and 200MPa)
S<1mm2 (3 axis)

Area ÷4 vs SoA

Nanobeams

3-axis gyroscope

F_0 ≈ 20.3 kHz
Q > 100.000 S=0.8mm² / axis

P.Robert et al, 2009 IEEE Sensors
D.Ettelt et al, 2011 Transducers

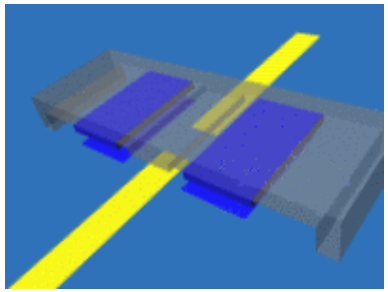
3D magnetometer

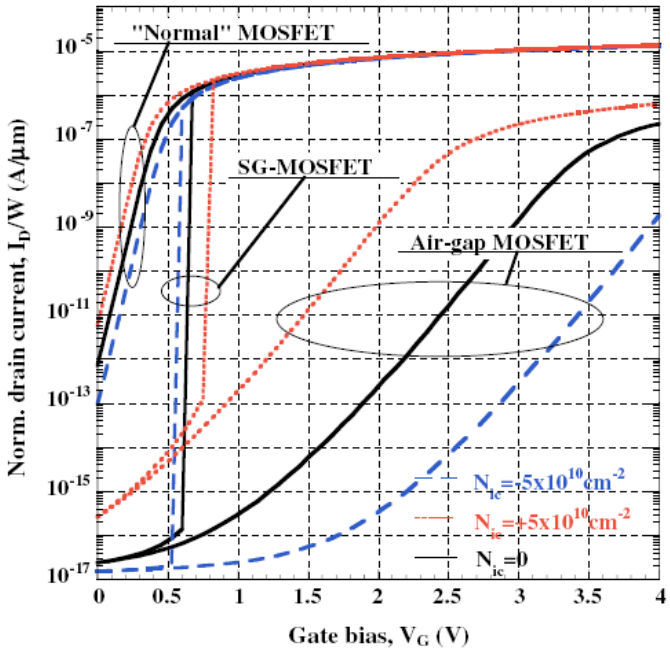
Resol 20-80 nT/√Hz
Lin 4.5 mT
S=0.25 mm²/axis

microphone

pressure sensor

NEMS switches





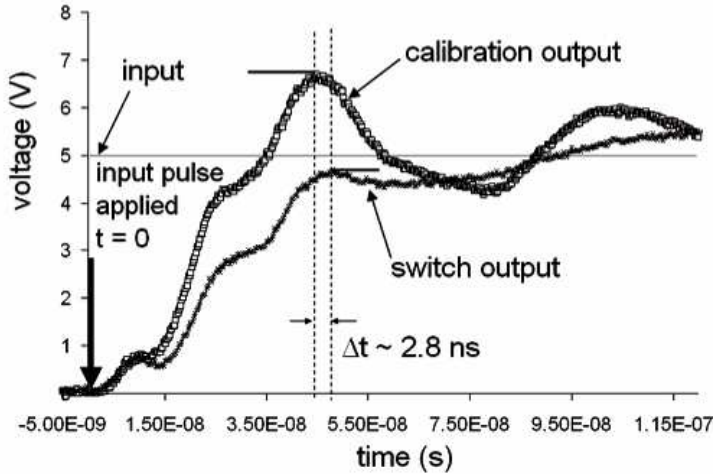
from D. Tsamados et al. Solid-State Elec. 52 1374 (2008)

high on/off ⇒ low power logic

“high” speed

⇓

rf

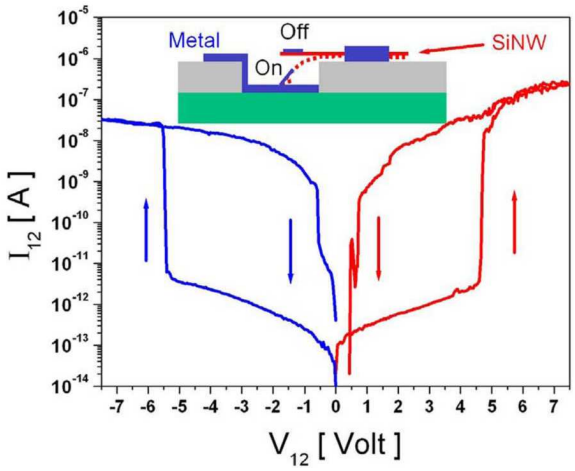


from AB. Kaul et al., Nano Letters 6(5) 942-947 (2006)

bistable

⇓

memory



from Q.Li et al.,IEEE Nano 6(2) 256-262 (2007)

Conclusion :
Nanoelectronics CMOS
from Devices to Systems Perspectives

- Innovation from strong association
  System/Device/Materials Science and Engineering
- Si CMOS: Nanoelectronics Base platform beyond ITRS
- Low Power consumption: major challenge (sub 1V VDD CMOS).
  => Device/ system architecture optimization
  (GAA nanowires, low slopes,design, 3D)
  => Opportunities for new materials
  (revised low BG III-V, Carbon)
- Heterogeneous 3D co-Integration on Si, Low Power:
  Add Functionalities for diversification. NonCMOS & CMOS
  Monolithic, 3rd dimension in device,
  Stacked mixed functions, System On Wafer
- Durable Low Power solutions:
  health, environment, quality of life, IST,…

Acknowledgements

- Professors Hiroshi Iwai and Shunri Oda, Tokyo Institute of Technology
- Organization committee of the International Symposium on Advanced Hybrid Nano Devices
- Colleagues of CEA LETI especially Eric Ollier, Cécilia Dupré, Thomas Ernst.

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Merci de votre attention

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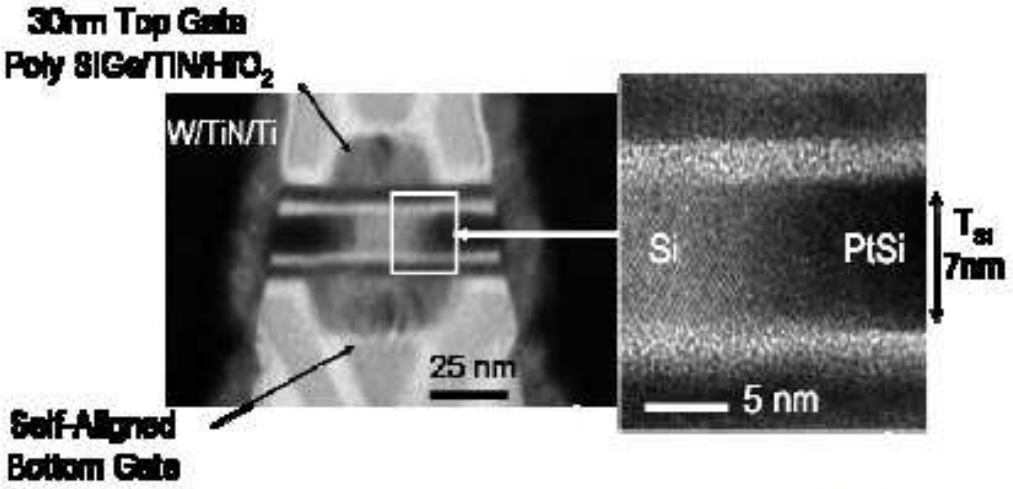
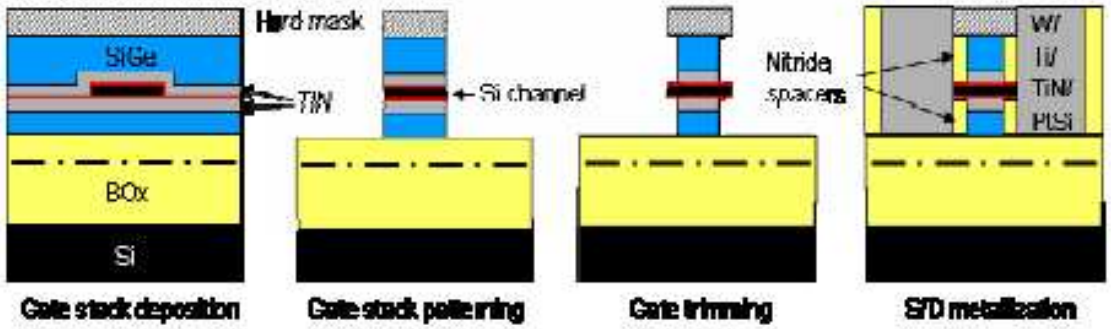
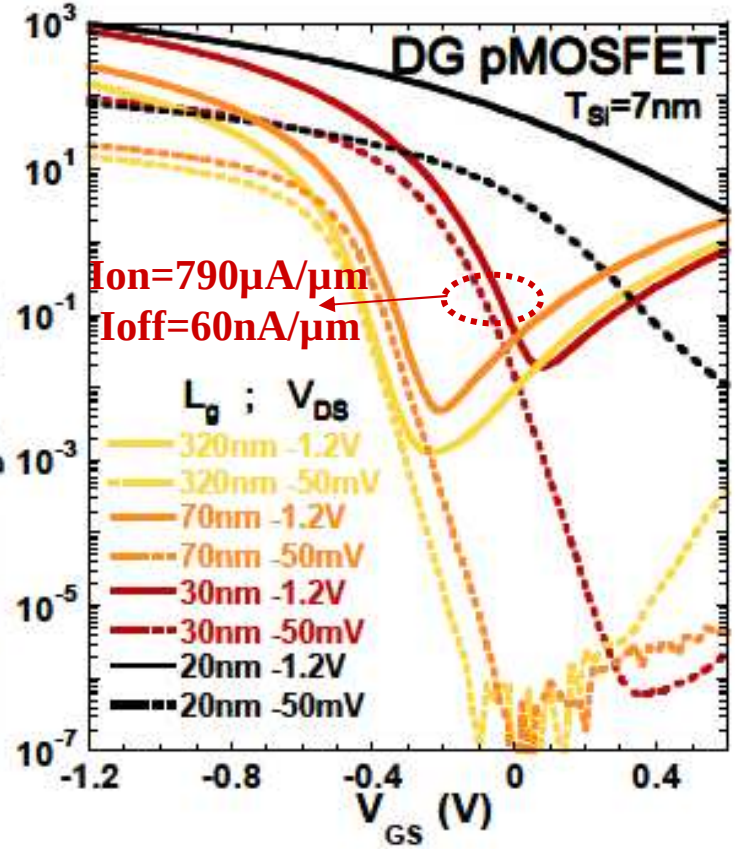
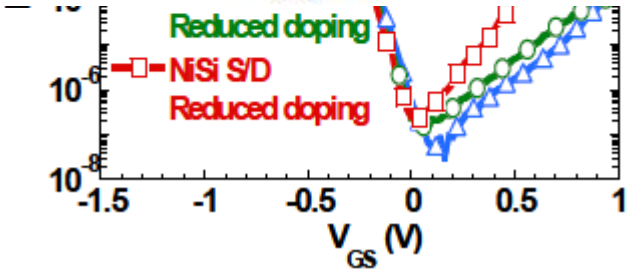
Dual Schottky MOSFET (Dopant Segregated S/D)

Reduce series resistance to channel









Still Dopant Segregation necessary:

Junctionless FET(JP Colinge)?

Process simplicity vs. RDF, VT adjust

Application Drivers

MOBILE WIRELESS | CONSUMER | HEALTH | COMPUTING & STORAGE | AUTOMOTIVE

Form Factor

Ultra small TV Tuner , Sharp

Computer control using the

Cost

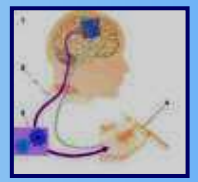
128 GB SSD, Toshiba

Great focus on packaging & integration to follow historic drivers

Performance

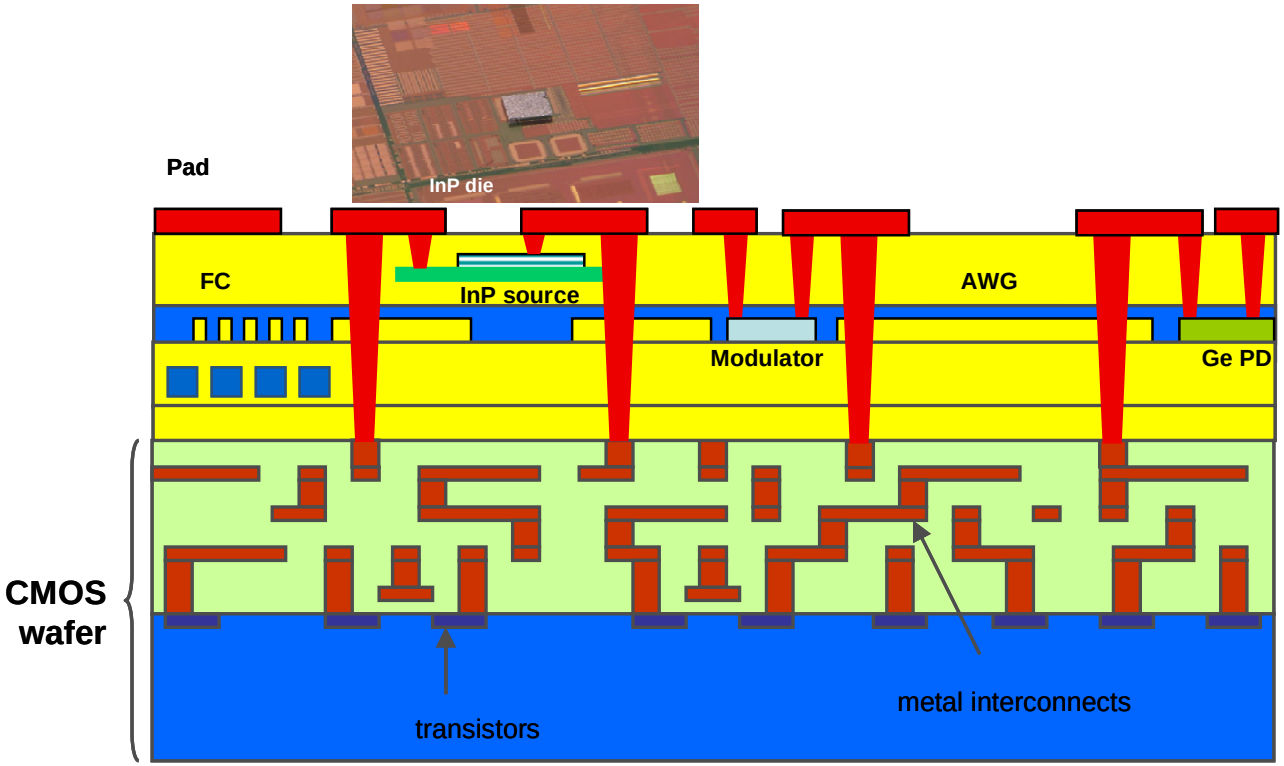
Nokia N82, 5Mpixel Video capture, coding, transmission

One Chip SetTopBox (STM)

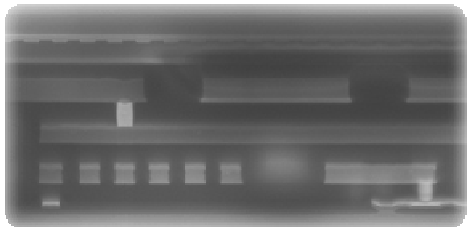


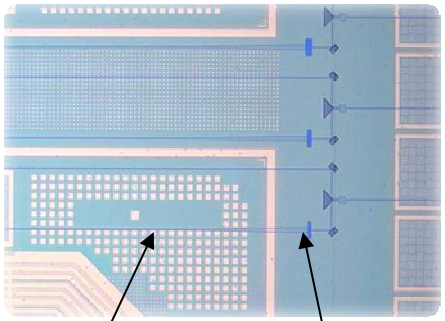
Intel's Teraflop Chip

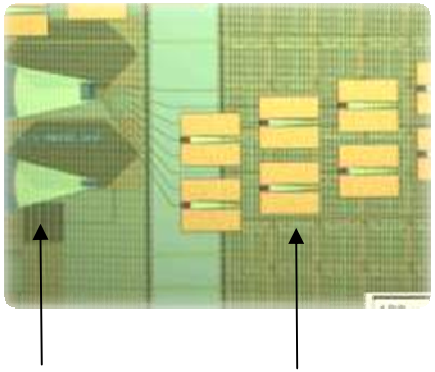
Silicon Photonics building blocks. 3D Integration

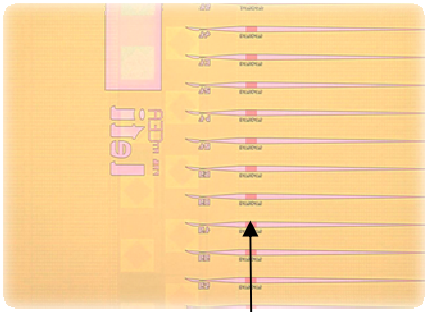


- 3D integration
- Not depending on the specific node used to produce the electronic wafer

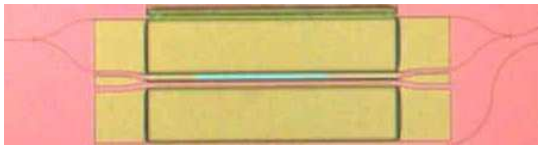




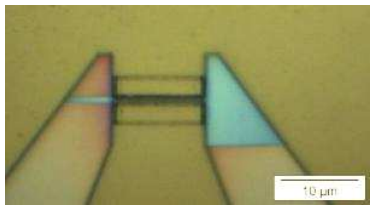




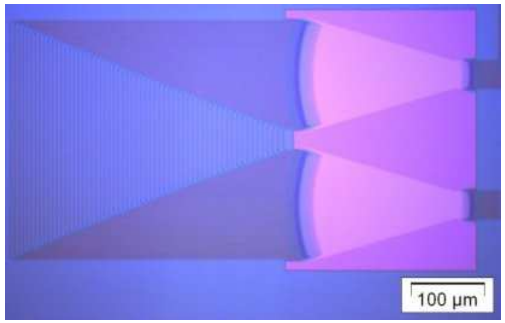
Photonics Integration on Silicon.
The building blocks.



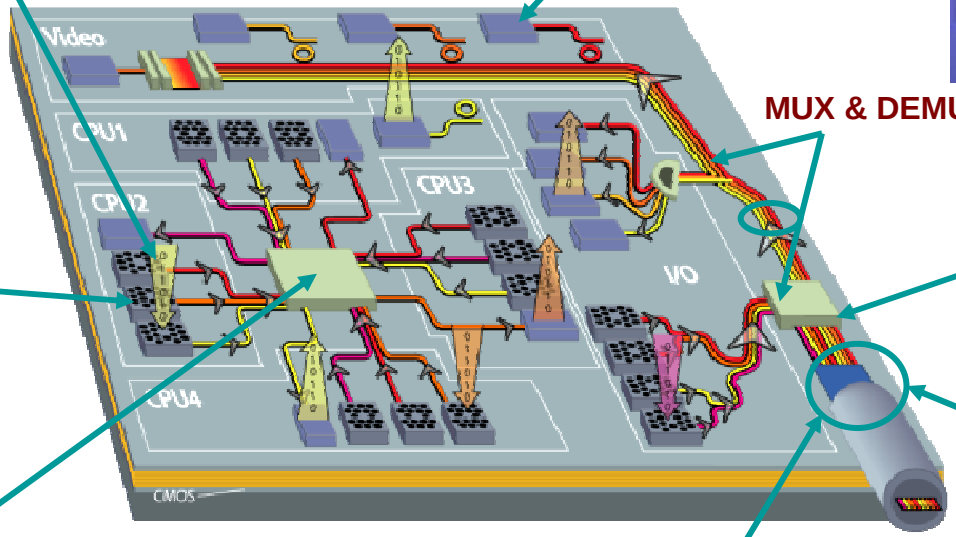
Optical modulator

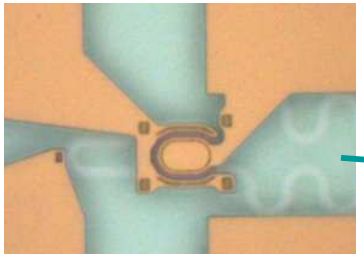


Photodetector



MUX & DEMUX





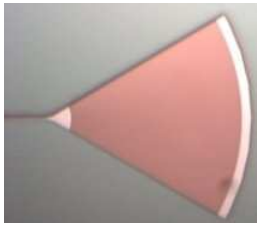
Laser source

Waveguide

Grating coupler

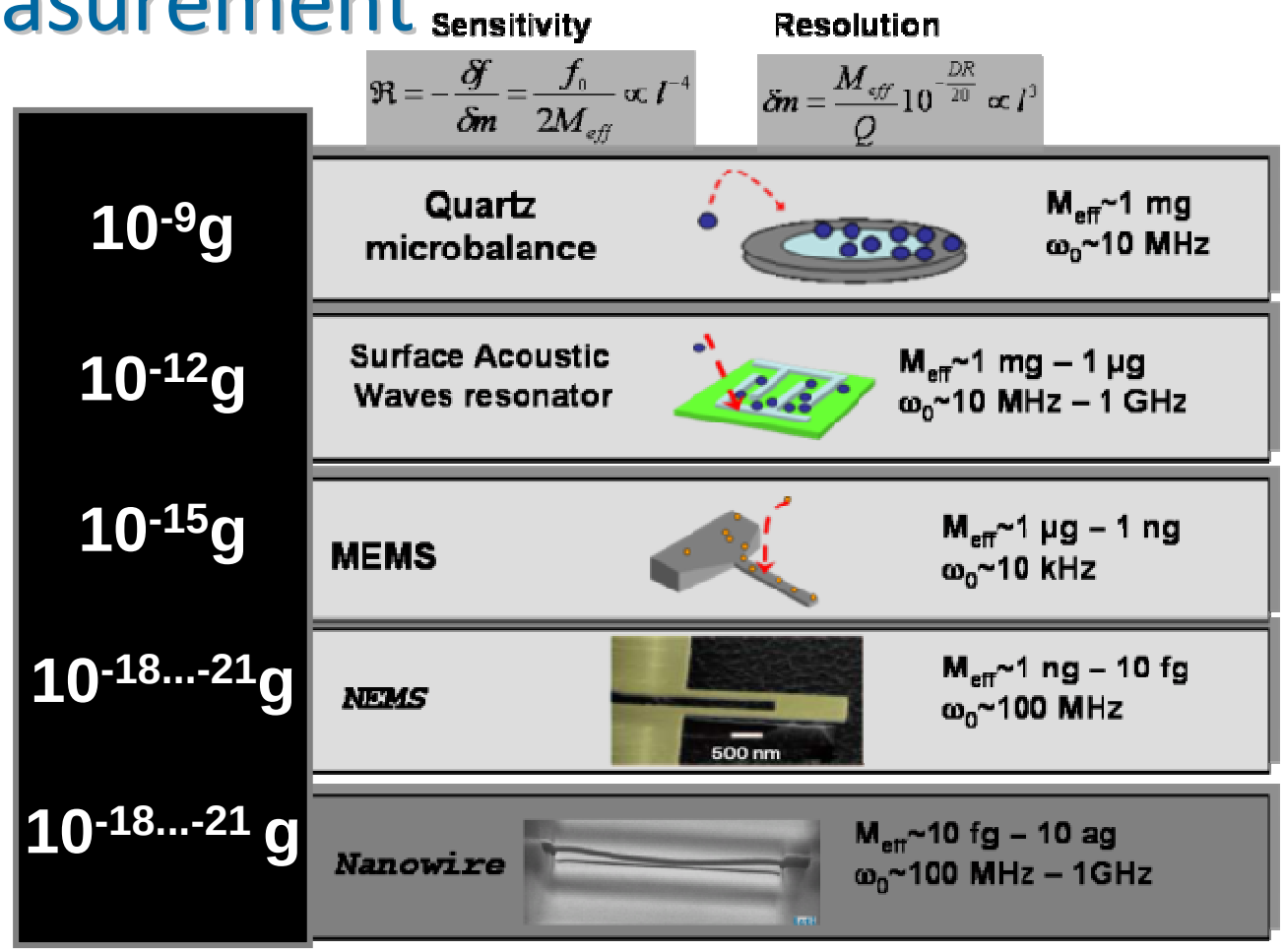
Optical switch

In-plane coupler



LETI: L.Fulbert ESSDERC 2011

Nanowires for very sensitive mass measurement



T. Ernst et al., IEDM 08

Few molecules sensitivity can be achieved => 1zg